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SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides installation, operation and maintenance instructions for the Model 1616 Magnetic Tape Interface Subsystem.

1.2 REFERENCES

1. Magnetic Tape Formatter Manual
2. UNIVAC 1616 Processor Handbook

1.3 PURPOSE OF EQUIPMENT

The Model 1616 Magnetic Tape Interface Subsystem (MTS) is a complete magnetic tape storage subsystem designed for use in conjunction with the UNIVAC Model 1616 Computer.

The MTS performs all functions required to read or write IBM compatible tapes. Depending upon user specifications, the MTS can operate 7-track tape drives at 200, 556, or 800 BPI, and/or 9-track tape drives at 800 BPI NRZI, or 1600 CPI phase encoded.

The Model 1616 Magnetic Tape Subsystem consists of a Magnetic Tape Formatter and a 1616 Interface printed-circuit board. The formatter comprises a chassis suitable for mounting in a standard 19-inch RETMA rack. Within the chassis are: (1) the formatter PCB; (2) the 1616 Interface PCB; (3) a mother board; and (4) a power supply. The formatter, power supply and mother board are covered in the Formatter Manual.

The 1616 Interface is a single PCB that measures 16.75 inches by 11.95 inches. This PCB has one edge-type connector (P7). Connector P7 is a dual edge-type, 35-pin PCB connector designed to mate with a Masterite connector 37GR35-DR-H-X, or equivalent. Connector P7 plugs into the mother board and is used for communication with the formatter PCB. There are also two connectors on the PCB (XP1 and XP2) which are wired to rear panel connectors IN1 and OUT1, respectively.

SECTION II

INSTALLATION AND OPERATION

2.1 GENERAL

Both the MTS and the tape transport(s) are generally mounted in a standard 19-inch rack. Installation consists of mounting the two units, connecting the input/output cables between the UNIVAC 1616 and the MTS and connecting cables between the MTS and each tape transport.

General instructions for installation and operation of the formatter are given in the Formatter Manual. The Interface PCB is installed in the formatter at the factory and, therefore, the only additional installation information required is that of interconnecting the MTS and the UNIVAC 1616.

2.2 INTERFACE CHARACTERISTICS

Figure 2-1 shows the configuration of the transmitters and receivers. The interface circuits are designed so that a disconnected wire results in a false signal.

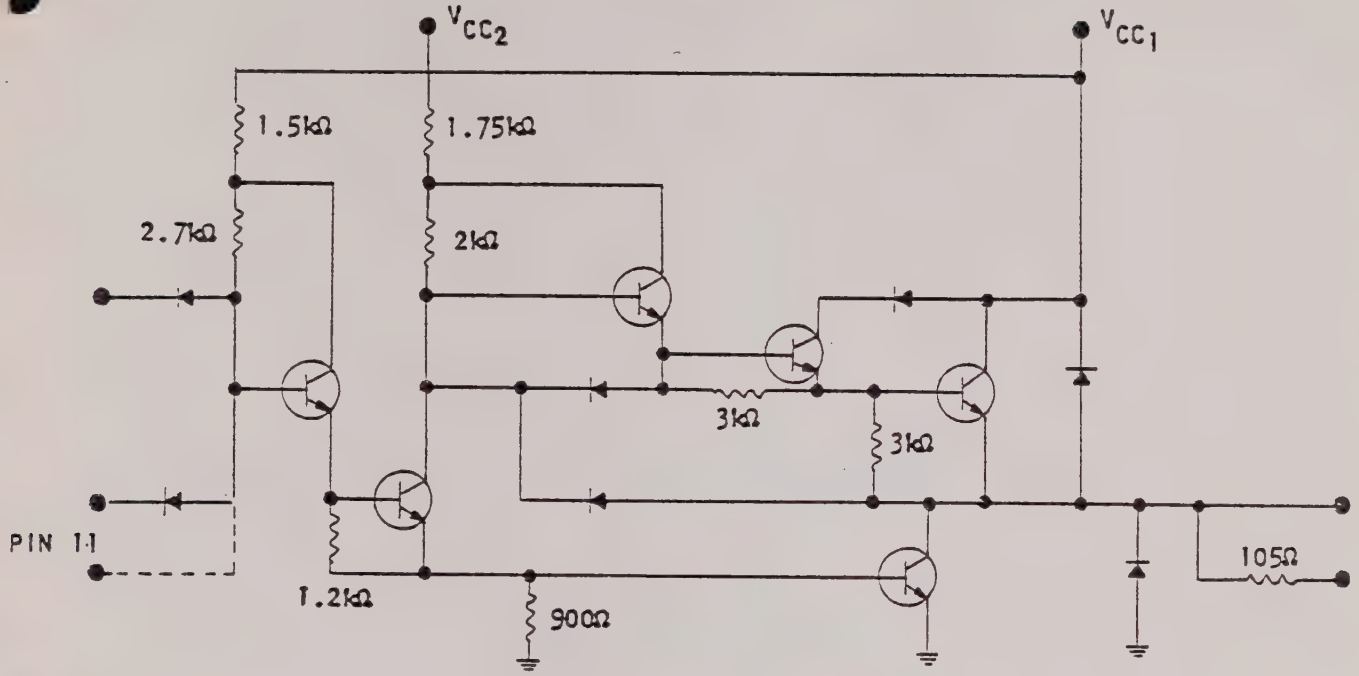
The logic levels are:

1. -3 Volt Interface (NTDS Fast)

Receivers -	True	=	High	= 0 Volt (approx.)
	False	=	Low	= -3 Volts
Drivers -	True	=	Low	= 0 Volt (approx.)
	False	=	High	= +4.0 Volts

SCHEMATIC DIAGRAM (ONE SIDE ONLY)

9621 LINE DRIVER



EQUIVALENT CIRCUIT

9622 LINE RECEIVER

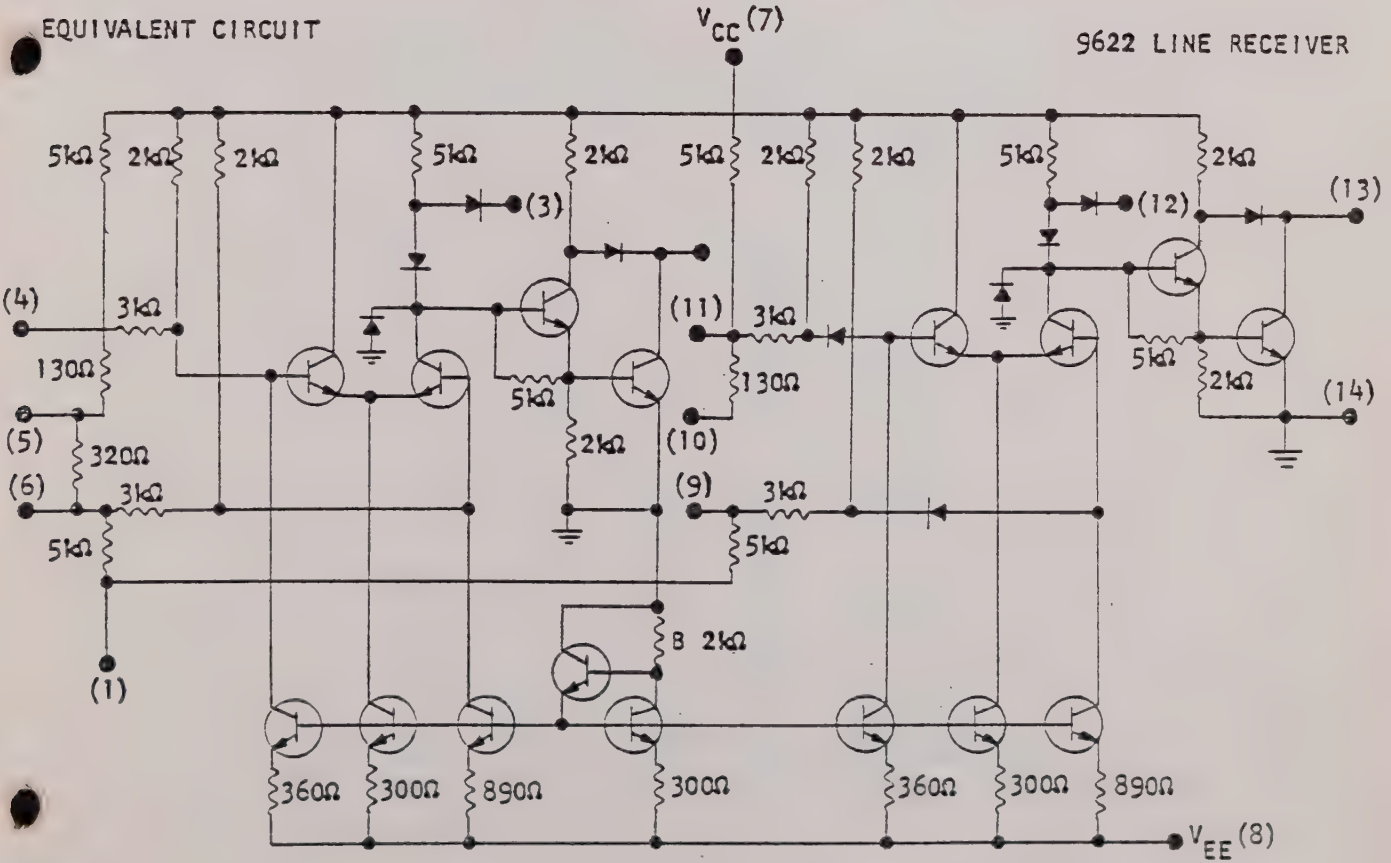


Figure 2-1. Interface Configuration

2. +3 Volt Interface (ANEW)

Receivers - True = Low = 0 Volt (approx.)
False = High = +3.5 Volts

Drivers - True = Low = 0 Volt (approx.)
False = High = +4.0 Volts

2.3 INTERCONNECTION

Tables 2-1 and 2-2 list the signals exchanged between the MTS and the UNIVAC 1616.

Table 2-1
UNIVAC 1616 To MTS Signals

PICO OUT 1	-3 Volts Interface	+3 Volts Interface	Mnemonic	Signal Definitions
1	G4	H4	ODB15	Output Data Bit 15 (MSB)
11	H4	G4	RET	Return
2	G3	H3	ODB14	Output Data Bit 14
12	H3	G3	RET	Return
4	G2	H2	ODB13	Output Data Bit 13
14	H2	G2	RET	Return
3	G1	H1	ODB12	Output Data Bit 12
13	H1	G1	RET	Return
6	D12	C12	ODB11	Output Data Bit 11
16	C12	D12	RET	Return
5	D11	C11	ODB10	Output Data Bit 10
15	C11	D11	RET	Return
34	D10	C10	ODB09	Output Data Bit 09
24	C10	D10	RET	Return
33	D9	C9	ODB08	Output Data Bit 08
23	C9	D9	RET	Return

Table 2-1

UNIVAC 1616 To MTS Signals (Cont'd)

PICO OUT 1	-3 Volts Interface	+3 Volts Interface	Mnemonic	Signal Definitions
35	D8	C8	ODB07	Output Data Bit 07
25	C8	D8	RET	Return
36	D7	C7	ODB06	Output Data Bit 06
26	C7	D7	RET	Return
31	D6	C6	ODB05	Output Data Bit 05
21	C6	D6	RET	Return
32	D5	C5	ODB04	Output Data Bit 04
22	C5	D5	RET	Return
40	D4	C4	ODB03	Output Data Bit 03
30	C4	D4	RET	Return
39	D3	C3	ODB02	Output Data Bit 02
29	C3	D3	RET	Return
38	D2	C2	ODB01	Output Data Bit 01
28	C2	D2	RET	Return
37	D1	C1	ODB00	Output Data Bit 00 (LSB)
27	C1	D1	RET	Return
7	B5	A5	OUT DATA ACK	Output Data Acknowledge
17	A5	B5	RET	Return
8	A7	B7	EXT FUNC ACK	External Function Acknowledge
18	B7	A7	RET	Return
9	A6	B6	OUT DATA REQ	Output Data Request
19	B6	A6	RET	Return
10	A8	B8	EXT FUNC REQ	External Function Request
20	B8	A8	RET	Return
20	A1	A1		Shield Ground

Table 2-2

MTS To UNIVAC 1616 Signals

PICO IN 1	-3 Volts Interface	+3 Volts Interface	Mnemonic	Signal Definitions
7	H4	G4	IDB15	Input Data Bit 15 (MSB)
17	G4	H4	RET	Return
8	H3	G3	IDB14	Input Data Bit 14
18	G3	H3	RET	Return
5	H2	G2	IDB13	Input Data Bit 13
15	G2	H2	RET	Return
6	H1	G1	IDB12	Input Data Bit 12
16	G1	H1	RET	Return
4	C12	D12	IDB11	Input Data Bit 11
14	D12	C12	RET	Return
3	C11	D11	IDB10	Input Data Bit 10
13	D11	C11	RET	Return
38	C10	D10	IDB09	Input Data Bit 09
28	D10	C10	RET	Return
37	C9	D9	IDB08	Input Data Bit 08
27	D9	C9	RET	Return
40	C8	D8	IDB07	Input Data Bit 07
30	D8	C8	RET	Return
39	C7	D7	IDB06	Input Data Bit 06
29	D7	C7	RET	Return
36	C6	D6	IDB05	Input Data Bit 05
26	D6	C6	RET	Return
35	C5	D5	IDB04	Input Data Bit 04
25	D5	C5	RET	Return
33	C4	D4	IDB03	Input Data Bit 03
23 1	D4	C4	RET	Return
34	C3	D3	IDB02	Input Data Bit 02
24	D3	C3	RET	Return
31	C2	D2	IDB01	Input Data Bit 01
21	D2	C2	RET	Return

Table 2-2

MTS To UNIVAC 1616 Signals (Cont'd)

PICO IN 1	-3 Volts Interface	+3 Volts Interface	Mnemonic	Signal Definitions
32	C1	D1	IDB00	Input Data Bit 00
22	D1	C1	RET	Return
11	B8	A8	EIE	External Interrupt Enable
1	A8	B8	RET	Return
12	B6	A6	IN DATA ACK	Input Data Acknowledge
2	A6	B6	RET	Return
9	A7	B7	EXT INT REQ	External Interrupt Request
19	B7	A7	RET	Return
10	A5	B5	IN DATA REQ	Input Data Request
20	B5	A5	RET	Return
21	A1	A1		Shield Ground

To interconnect the equipment, proceed as follows:

WARNING

Prior to initiating this procedure, insure that power to the computer and to the MTS is OFF to avoid injury to personnel and/or damage to the equipment.

1. Plug the 1616 input connector into the COMPUTER IN1 connector on the MTS rear panel.

2. Plug the 1616 output connector into the COMPUTER OUT1 connector on the MTS rear panel.

The equipment is now ready for operating and checkout as described in the Formatter Manual.

SECTION III
INTERFACE LOGIC

3.1 INTRODUCTION

The interface logic is shown on Drawing 88003.

Each mnemonic shown on the logic diagrams has a number or numbers next to it. These numbers indicate either the sheet of origin or the destination of the signals. Throughout this discussion, logic elements which cannot be identified by mnemonic are called out according to their location on the printed-circuit board and output pin number. For example, an inverter in location B5 with its output on pin 8 is identified as inverter B5-8.

A block diagram of the interface is shown in Figure 3-1.

The interface printed-circuit board in the magnetic tape subsystem (MTS) is connected to the computer by two twisted-pair shielded cables; one for input and the other for output. Unless otherwise specified, input is defined as input to the computer and output as output from the computer. There are four control lines and sixteen data lines in each cable.

Four categories of signals are exchanged between the computer and the MTS:

1. Control Signals
2. Data
3. Status (from MTS to Computer)
4. External Function Commands (from Computer to MTS)

The methods used to accomplish these exchanges are discussed in the following paragraphs.

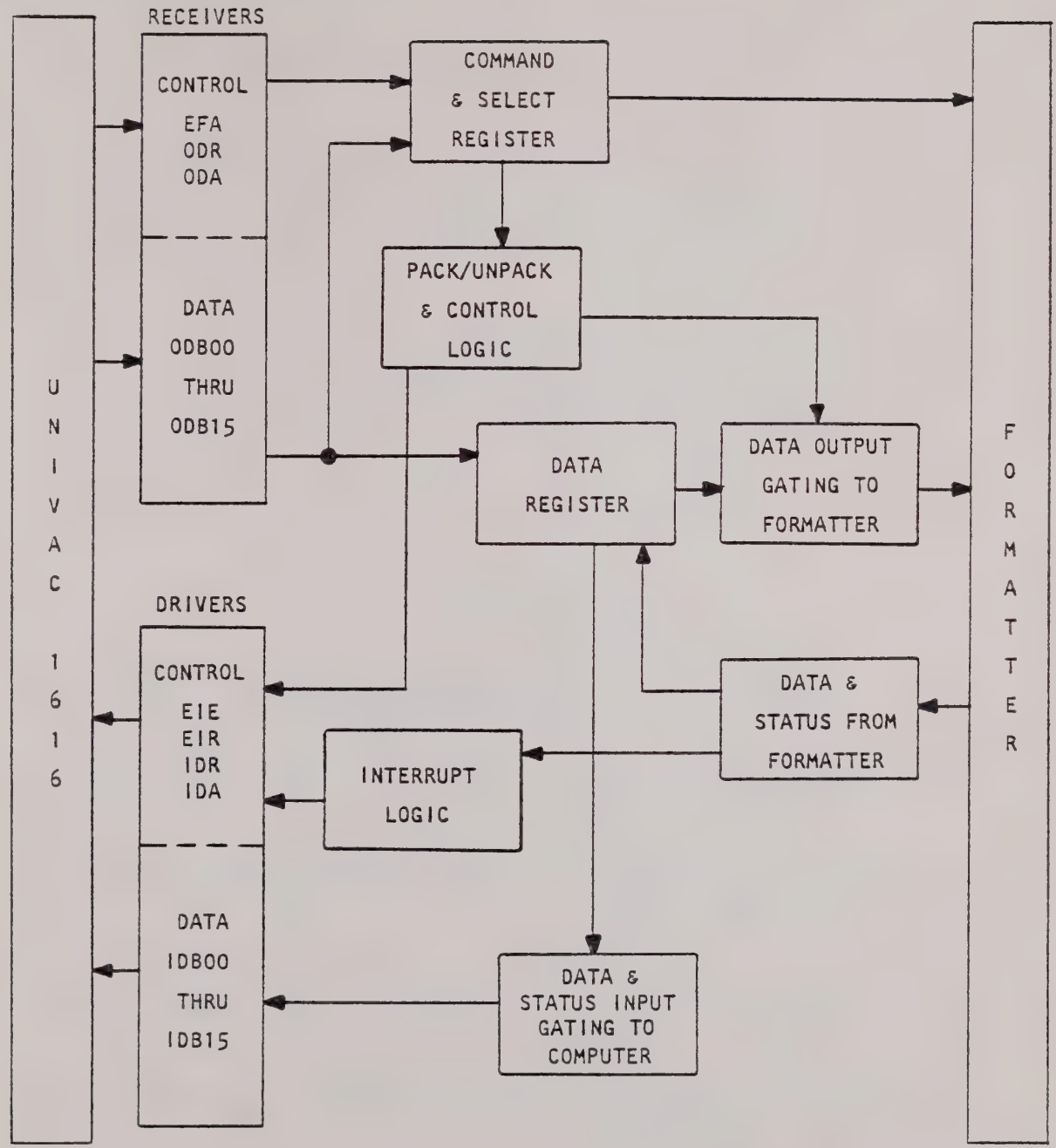


Figure 3-1. UNIVAC 1616 Interface Block Diagram

3.2 CONTROL LINES (Sheets 4, 21 & 27)

The eight control lines are divided into two groups of four lines each. One group functions with the output channel; the other group functions with the input channel. The functions of each group are shown in Tables 3-1 and 3-2, respectively.

Initiation of any information exchange between the Computer and the MTS must be started by the Computer, placing an external function command on the output data (OD) lines and then setting the External Function Acknowledge (EFA) line.

Table 3-1
Output Channel Control Lines

Line	Signal Direction	Function
External Function Request (EFR)	MTS to Computer	True condition indicates that MTS is ready to accept external function code word.
External Function Acknowledge (EFA)	Computer to MTS	True condition indicates that Computer has placed external function code on output data lines.
Output Data Request (ODR)	MTS to Computer	True condition indicates that MTS is ready to accept a data word.
Output Data Acknowledge (ODA)	Computer to MTS	True condition indicates that Computer has placed data word on output data lines.

Table 3-2

Input Channel Control Lines

Line	Signal Direction	Function
External Interrupt Enable (EIE)	Computer to MTS	True condition indicates that Computer will accept an interrupt (not used in this application).
Input Data Request (IDR)	MTS to Computer	True condition indicates that MTS has placed data word on input data lines to Computer.
External Interrupt Request (EIR)	MTS to Computer	True condition indicates completion of an operation or an error. Status word is placed on input data lines.
Input Data Acknowledge (IDA)	Computer to MTS	True condition indicates that Computer has sampled the input data lines.

Each output channel control line is brought into the MTS through connector P1 into the negative side of a dual-line receiver. The positive side of the receiver serves as the signal return. The output channel control signals from the Computer are 0 Volts to produce a binary "1" (+5 Volts) output from the receiver and -3 Volts to produce a binary "0" (0 Volts) at the receiver output.

The input channel control lines from the MTS to the Computer are driven by dual-line drivers that provide outputs of 0 Volts for a binary "1" and +5 Volts (nominal) for a binary "0". These signals are put on the input data (ID) lines through connector P2.

3.3 I/O SEQUENCE

The input/output sequence of events for the various control line functions are discussed in following paragraphs.

3.3.1 External Function Request

The signal direction on this line is from the MTS to the Computer. The signal on this line is always high (false) and, therefore, external function commands to the MTS are "forced" under program control. The sequence is as follows:

1. The Computer places the function command on the OD lines.
2. The Computer sets the EFA line to indicate that the external function word is on the lines.
3. The MTS detects the setting of EFA and samples the code word.
4. The Computer clears the EFA line before placing the next word on the OD lines.

3.3.2 Output Data Request

The transfer of output data is controlled by the ODR line from the MTS to the Computer. The sequence is as follows:

1. When the MTS is ready to accept data, it sets the ODR line.
2. In accordance with internal priorities, the Computer detects the setting of ODR.
3. The Computer places a data word on the OD lines.
4. The Computer sets the ODA line to indicate that a word is present on the OD lines.
5. The MTS detects the setting of ODA, samples the data and clears ODR.
6. The Computer clears the ODA line before placing the next word on the OD lines.

3.3.3 External Interrupt Request

The EIR signal is sent to the Computer at the completion of each operation. It is sent immediately if a Rewind command has been received and another tape transport can be selected immediately. The sequence of events is as follows:

1. Upon completion of an operation, the MTS places the status word on the ID lines.
2. The MTS sets EIR to indicate that the status word in on the lines.
3. In accordance with internal priorities, the Computer detects the setting of EIR.
4. The Computer samples the status word and then sets IDA.
5. The MTS clears EIR.
6. The Computer must clear IDA before sampling the next word on the input data lines.

3.3.4 Input Data Request

The transfer of data from the MTS to the Computer is controlled by the IDR line. The sequence is as follows:

1. The MTS places a data word on the ID lines.
2. The MTS sets the IDR line to indicate that a data word is on the input data lines.
3. In accordance with internal priorities, the Computer detects the setting of IDR.
4. The Computer samples the data word and then sets IDA to indicate that the data has been sampled.
5. The MTS detects the setting of IDA and clear IDR.
6. The Computer clears IDA before sampling the next word on the ID lines.

3.4 DATA LINES (Sheets 1-3 & 25-27)

Data is exchanged over the 32 input/output lines using pack/unpack logic located on the Interface PCB. The pack/unpack logic provides compatability with UNIVACs' modulus selection for 16-bit Computer configurations using either 6 or 8-bit recording formats. There are 16 output data lines (connector P1) and 16 input data lines (connector P2). The data receiver and driver characteristics are identical to those of the control line drivers and receivers.

The data word formats for the Computer, 7-track magentic tape and 9-track magnetic tape are shown in Figures 3-2, 3-3 and 3-4, respectively.

3.5 STATUS WORD

The status word is placed on the input lines by the MTS upon completion of each operation or upon receipt of a Read Status command. The status bits are defined in Table 3-3.

3.6 COMMAND WORD

Command words are transferred to the MTS under control of the Computer when it sets the EFA line. In this application, the MTS EFR line is held false (high) and the external function command is a "forced" operation under program control.

The command word format is shown in Figure 3-5.

3.7 COMMAND AND SELECT REGISTER (Sheets 5 & 6)

The command and select register stores and decodes the four low-order bits of the external function command. These bits determine the type of operation to be performed by the MTS. It also contains the logic required for tape drive addressing and for selecting density, parity, 7 or 9-track and, in the case of dual-deck systems, NRZI or phase encoded operation.

3.7.1 Tape Drive Addressing

The MTS can operate up to four tape drives. These drives can be 7-track at 200, 556 or 800 BPI, and/or 9-track at 800 BPI NRZI in any combination. Provision is also made for handling dual-density drives which allow for either NRZI (800 BPI) or phase-encoded operation (1600 CPI).

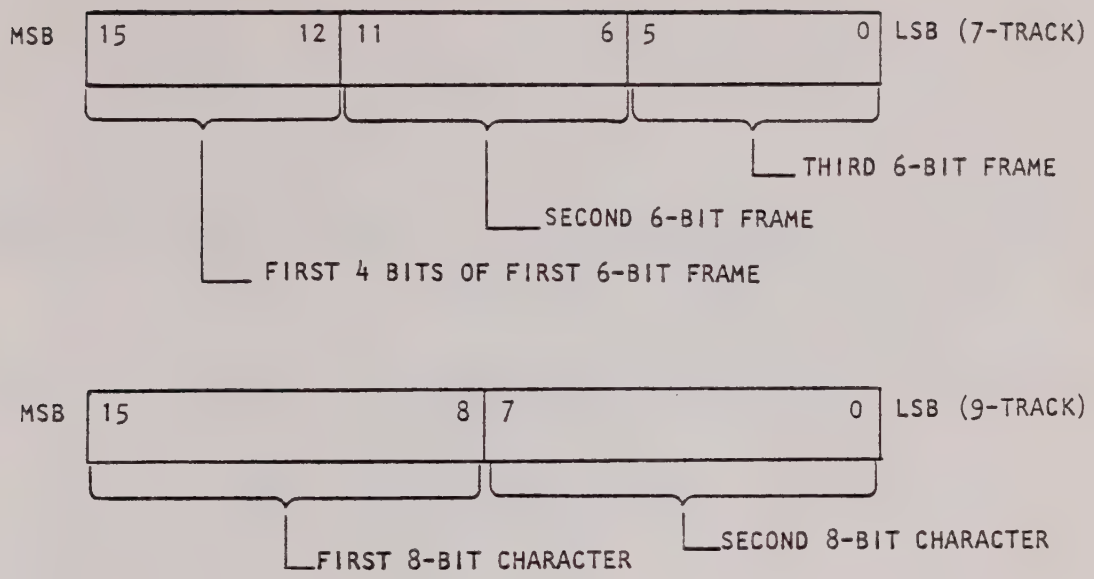


Figure 3-2. Computer Word Format

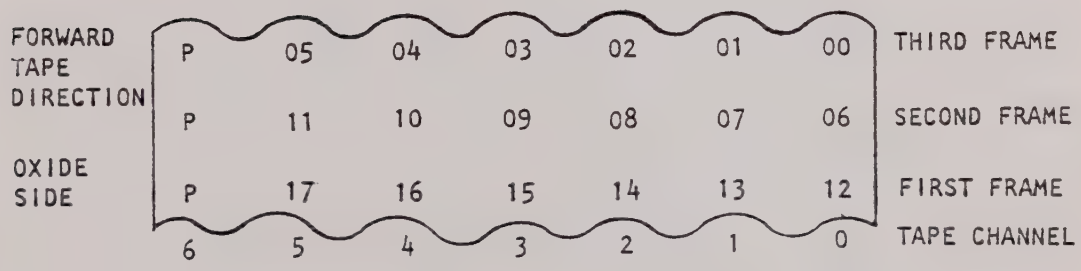

FORWARD TAPE DIRECTION
OXIDE SIDE
P 05 04 03 02 01 00
THIRD FRAME
P 11 10 09 08 07 06
SECOND FRAME
P 17 16 15 14 13 12
FIRST FRAME
6 5 4 3 2 1 0
TAPE CHANNEL

Figure 3-3. Seven-Track Tape Format

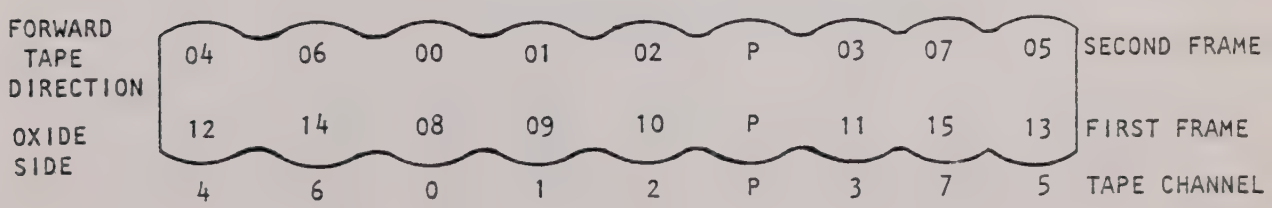
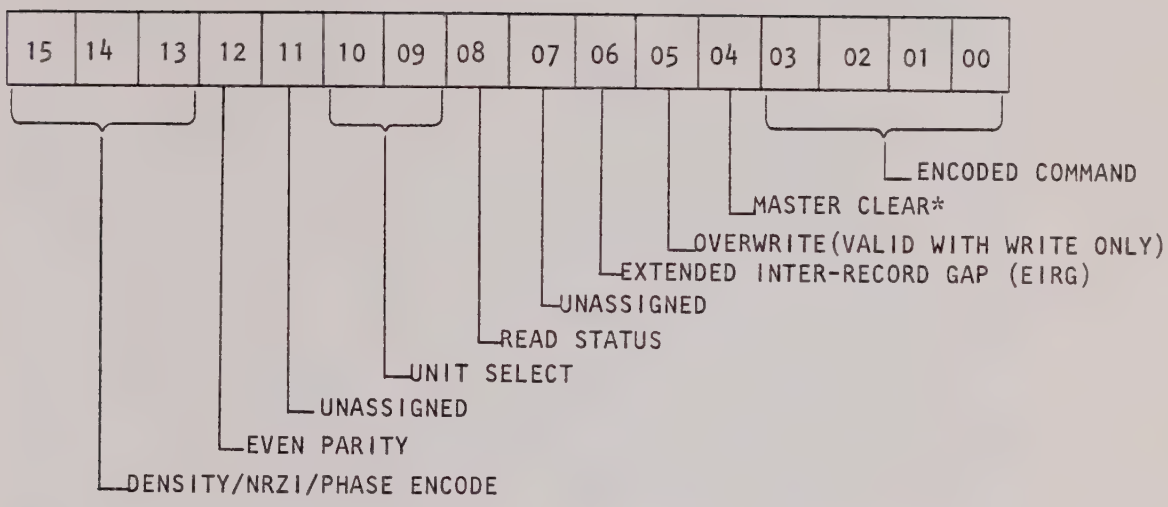

FORWARD TAPE DIRECTION
OXIDE SIDE
04 06 00 01 02 P 03 07 05
SECOND FRAME
12 14 08 09 10 P 11 15 13
FIRST FRAME
4 6 0 1 2 P 3 7 5
TAPE CHANNEL

Figure 3-4. Nine-Track Tape Format

Table 3-3

Status Bits

Computer Bit	Status Bit	Description
0	EF	Error Flag-set if EOT, parity error, or reject is set at end of operation.
1	EOT	End-of-Tape-set at detection of EOT until Rewind or Backspace is executed.
2	BOT	Beginning-of-Tape.
3	RWG	Rewinding.
4	FM	File Mark.
5	PE	Parity Error-one or more parity errors detected in last record. Checks for old character parity and even longitudinal parity for each track.
6	OFL	Offline-selected unit is offline.
7	RJT	Reject-command was not valid. 1. Write command issued and no write ring installed on tape unit. 2. Backspace at BOT. 3. Controller busy and any command other than read status issued. 4. Tape unit offline. 5. Command is NO Operation.
8	ODD	Odd number of tape characters read in last record. Program should strip off even characters of last word since it is meaningless.
9	CBUSY	Controller is busy.
10	TG	Tape Gap.
11	FP	Selected unit is file protected.
12-15		Unassigned.



*MASTER CLEAR will return current status

Figure 3-5. Command Word Format

Receiver output bits CID09 and CID10 are used to address the desired drive. These bits, which must be refreshed with each command, are applied to two flip-flops in location E13. The flip-flops are clocked by the trailing edge of delayed parameter clock, STCLK, which goes high at the same time as CMDCLK and returns low approximately 160 nanoseconds later. The outputs of these flip-flops are gated to provide address selection signals $\overline{\text{ESE01}}$ through $\overline{\text{ESE04}}$. Unit selection is as follows:

CID Bits 10	09	ESE Bits 01	02	03	04	Unit Selected
0	0	0	1	1	1	0
0	1	1	0	1	1	1
1	0	1	1	0	1	2
1	1	1	1	1	0	3

The $\overline{ESE}$ signals are supplied to the formatter board through connector P7 and to the jumper block shown at the bottom of Sheet 6. If a jumper is installed for the addressed unit, the low $\overline{ESE}$ signal causes the output of OR-Gate C15-8 to go high which, in turn, causes $\overline{E9TRK}$ to go high and $\overline{E7TRK}$ to go low. This indicates that a 7-track unit has been addressed. Conversely, if the selected unit has not been jumpered, the output of OR-Gate C15-8 remains low, indicating that a 9-track unit has been addressed. The signals are sent to the formatter through connector P7 and are also used in the logic on Sheet 5 to generate gating signals for the pack/unpack buffer logic. The addressed unit responds to the formatter with its status and the formatter, if ready, supplies a tape controller and formatter ready signals ($\overline{ETPCR}$ low, Sheet 19) to the interface.

3.7.2 Density, Dual Density NRZI/Phase Encode Selection

The selection of density, and dual-density, NRZI/Phase Encode operation is controlled by bits CID13 through CID15 and the jumper arrangement shown at the bottom of Sheet 6.

If the tape drives are all NRZI, a jumper is installed between pins 7 and 8 on the jumper block. This disables NAND-Gate A15-3 and density selection is then dependent upon the outputs of OR-Gate C15-8 and the LODN and 8HI flip-flops. If a 7-track unit is addressed, the output of the OR-Gate is high and both NAND-Gates A15-11 and A15-6 are enabled. Density selection is then as follows:

CID Bits 14	13	Density Selected
0	0	800 BPI
0	1	556 BPI
1	1	200 BPI

If a 9-track unit is addressed, the output of OR-Gate C15-8 is low, thereby disabling NAND-Gates A15-11 and A15-6. $\overline{\text{LODN}}$ is then high and $\overline{\text{8HI}}$ is low. This combination selects 800 BPI high density.

If the drives are dual density, a jumper is installed between pins 6 and 9 on the jumper block. The reset output of the select phase encode flip-flop ($\overline{\text{SELPE}}$) is then used for NRZI or phase encode selection by controlling the state of $\overline{\text{LODN}}$. When the flip-flop is set, $\overline{\text{LODN}}$ is high. In this condition, phase encode is selected. When the flip-flop is reset, the output of NAND-Gate A15-3 pulls $\overline{\text{LODN}}$ low, thereby selecting NRZI. The setting or resetting of the flip-flop is dependent upon the state of bit CID15 when STCLK occurs.

3.7.3 Parity Selection

In 7-track operation, parity selection is determined by the state of flip-flop $\overline{\text{ODDP}}$. The flip-flop is controlled by bit CID12. With the flip-flop set, $\overline{\text{ODDP}}$ is high and even parity is selected. When the flip-flop is reset, odd parity is selected.

3.7.4 Read Status

Setting the read status flip-flop (RDSTAT) causes the status word to be placed on the ID lines. The flip-flop is controlled by bit CID08 and clocked by the negative-going edge of EFA. The status bits were defined in Table 3-3.

When the flip-flop is set, the high RDSTAT signal disables the reset signal (RSET, Sheet 11). The low $\overline{\text{RDSTAT}}$ signal generates a high input status signal (INPS, Sheet 22). The high INPS signal is gated with end-of-tape (EOT), parity error (PERE) and reject (RJT, Sheet 7) to set the error flag bit (EF) if applicable. INPS is also gated with the high inverse input data signal ($\overline{\text{INPD}}$) to provide the low external

interrupt signal (EIR, Sheet 21) which, in turn, sets the external interrupt request line (EXT INT REQ, Sheet 27). In addition, INPS enables the status word gates for the ID lines (Sheets 23 and 24).

The Computer, in response to the EXT INT REQ signal, samples the data on the ID lines and then sets the input data acknowledge (IN DATA ACK) line (Sheet 27). The high IDA signal and INPS cause the clear status signal ($\overline{\text{CLRSTAT}}$, Sheet 22) to go low. The low $\overline{\text{CLRSTAT}}$ signal resets the busy flip-flop (BSY) and the RDSTAT flip-flop. When RDSTAT resets, the INPS goes low, removing the EIR signal and the MTS is ready for a new command. Note that when a read status command is issued, STCLK is generated by leading edge function signal LEF and CID08 (Sheet 7), thereby eliminating the need for a CMDCLK signal.

The status word is placed on the ID lines at the end of each operation or in the event of an error. However, it may be requested by the Computer at any time although it would interfere with a normal read operation.

3.7.5 Command Register and Decode Logic

The command register and decode logic is shown on Sheet 5. The four low-order bits of the external function command define the type of operation to be performed by the MTS. These bits are brought into the MTS on pins D1 through D4, respectively, on connector P1 (Sheet 1) and applied to dual line receivers. Once the function command is on the OD lines, the Computer sets the EFA line to notify the MTS that the command is available.

The receiver outputs are designated CID00 through CID03. These signals are applied to storage register E12 (Sheet 5) which is clocked on the positive-going edge of inverse command clock signal, $\overline{\text{CMDCLK}}$. The outputs of the four storage register flip-flops associated with the encoded

bits are ID00 through ID03. These outputs are applied to a 4-to-10 line decoder. The decoder outputs (active low) for the various inputs are shown in Table 3-4.

The decoded $\overline{WT}$ and $\overline{RD}$ signals are gated with $\overline{E7TRK}$ and $\overline{E9TRK}$ to provide $\overline{7TW}$, $\overline{7TR}$, $\overline{9TW}$ and $\overline{9TR}$. These signals are used in the pack/unpack counter and control logic (Sheet 20) to gate data into or out of the data storage register.

Table 3-4
Decoder Outputs

ID Bits 03	02	01	00	Low Active Output Signal	Signal Definition
0	0	0	0	$\overline{NOOP}$	No Operation
0	0	0	1	$\overline{WT}$	Write
0	0	1	0	$\overline{WFM}$	Write File Mark
0	0	1	1	$\overline{RD}$	Read
0	1	0	0	$\overline{SPFR}$	Space Forward
0	1	0	1	$\overline{SPRV}$	Space Reverse
0	1	1	0	$\overline{SFSF}$	Start File Search Forward
0	1	1	1	$\overline{SFSR}$	Start File Search Reverse
1	0	0	0	$\overline{RWND}$	Rewind
1	0	0	1	$\overline{INV}$	Invalid

One other bit (CID06) is applied to the storage register but is not decoded. This is the extended inter-record gap bit (EIRG). Setting this bit causes an erasure of 3.75 inches to occur on the tape. At the end of the operation, the status word is placed on the ID lines and EIR is set to signal completion. This signal can also be used in conjunction with write to automatically provide the extended inter-record gap before command execution. The EIRG signal will be covered more fully in the discussion of the write operation.

3.8 FUNCTION COMMANDS

The logic operations required for each function command are discussed in the following paragraphs.

3.8.1 NO Operation

The NO operation command ($\overline{\text{NOOP}}$)contains all zeros in the four low-order bits. This command requires no action by the formatter and is treated as an illegal command in the interface logic.

The Computer, under program control places the command on the OD lines for a minimum of 3.2 microseconds and sets the EXT FUNC ACK line for a minimum of 2.2 microseconds. The EXT FUNC ACK signal notifies the MTS that data is available on the OD lines.

Setting the EXT FUNC ACK line causes external function acknowledge signal EFA and leading-edge function acknowledge signal LEF to go high (Sheet 4). EFA remains high as long as EXT FUNC ACK is set. LEF is a pulse approximately 130 nanoseconds wide, as determined by the logic elements and capacitor C2.

Refer to Sheet 7. EFA and $\overline{\text{CIDO8}}$ (read status bit not set) in conjunction with tape controller ready (TPCR) or rewind status (RWIG) generate command clock signal CMDCLK. TPCR and RWIG also provide a low $\overline{\text{TPIG}}$ signal which indicates that the tape controller is ready or rewinding and enables CMDCLK Gate A5-4. Another signal available to provide $\overline{\text{TPIG}}$ is the reset output of flip-flop H4. The function of this arrangement is to prevent "hanging up" the system in the event that the tape drive is rewinding or a non-existent tape drive has been addressed.

The high CMDCLK signal generates three 130 nanosecond pulses: a positive-going initialize command (INZX); a positive-going clock (CLK); and a negative-going clock ($\overline{\text{CLOCK}}$).

INZX is used to generate a low clear signal ($\overline{\text{CLR}}$, Sheet 10) which, in turn, provides a high clear signal (CLR). The low $\overline{\text{CLR}}$ signal is used to:

1. Reset data buffer full flip-flop, DBFL.
2. Reset input data enable flip-flop, INPD.
3. Provide a low register clear signal ($\overline{\text{REGCLR}}$, Sheet 7) which resets the command register (Sheet 5).
4. Reset the down ramp starting flip-flop (REND, Sheet 22).

The high CLR signal is used to:

1. Reset the external rewind command signal flip-flop (ERWD, Sheet 8).
2. Reset the odd character flip-flop (ODDC, Sheet 21).
3. Provides a low $\overline{\text{CLRSTAT}}$ signal which resets the busy and input status flip-flops (BSY and INPS, Sheet 22), the RDSTAT flip-flop (Sheet 6) and the reject flip-flop (RJT, Sheet 12).
4. Provide a high initialize signal (INTZ, Sheet 22) if $\overline{\text{TPCR}}$ is still high when CLR returns low. This signal is used on Sheet 12 to provide the external initialize ($\overline{\text{EINZT}}$) signal to the formatter.

The trailing edge of CLK sets flip-flop H4 on Sheet 7. The flip-flop is reset by a power-up reset command (PUP) which is high when bit CID04 and EFA are high (Sheet 9) or by $\overline{\text{RJT}}$ when the reject flip-flop is set. It is also reset when leading-edge tape controller ready signal ($\overline{\text{LTPR}}$) goes low.

The $\overline{\text{CLOCK}}$ signal generates delayed parameter clock signal STCLK which clocks the address, parity, density and NRZI/phase encode flip-flops on Sheet 6. It is also the clock for the external edit flip-flop ($\overline{\text{EEDIT}}$) on Sheet 8.

When the Computer resets the EXT FUNC ACK line, EFA goes low and $\overline{\text{CMDCLK}}$ goes high. The positive-going edge of $\overline{\text{CMDCLK}}$ clocks the CID00 through CID03 bits into the command storage register. The storage register outputs (ID00 through ID03) are applied to the 4-to-10 line decoder which provides a low-active output (in this case $\overline{\text{NOOP}}$) according to the decoded bits.

Refer to Sheet 7. The high EFA signal generates a 130 nanosecond external function acknowledge trailing edge signal ($\overline{\text{EFAT}}$). The positive-going trailing edge of $\overline{\text{EFAT}}$ causes the output of inverter C2-2 (Sheet 11) to go negative, clocking EFAT trailing edge flip-flop LEG set. Note that the inverted legal command signal ($\overline{\text{LEGL}}$) is prevented from going low by the low $\overline{\text{NOOP}}$ signal.

The low $\overline{\text{LEG}}$ signal in conjunction with the low output of NAND-Gate L5-8 and the low RDSTAT signal provide RSET (Sheet 11). The high RSET signal generates a 130-nanosecond reset pulse RSP (Sheet 22). $\overline{\text{RSP}}$ clocks the reject flip-flop (RJT, Sheet 12) set. It also generates $\overline{\text{REGCLR}}$ (Sheet 7) which clears the command register. RSP provides the external initialize signal (EINZT) to the formatter (Sheet 12).

RJT generates an error flag signal (EF) and $\overline{\text{RJT}}$ resets flip-flop H4, enabling the CMDCLK gating (Sheet 7). The low $\overline{\text{RJT}}$ also provides the input status signal (INPS) on Sheet 22. INPS and RJT are applied to a NAND-Gate on Sheet 24 which provides a low COD07 bit to inverter J11-2 on Sheet 26. The high inverter output causes the line driver output to go true.

The EF signal is applied, with INPS, to NAND-Gate H8-8 on Sheet 23 to provide a low $\overline{\text{COD00}}$ signal which causes the output of line driver L7-13 (Sheet 25) to go true.

The high $\overline{\text{INPD}}$ signal and INPS generate external interrupt request ($\overline{\text{EIR}}$, Sheet 21) which, in turn, provides the EXT INT REQ (Sheet 27) to the Computer. The Computer then samples the status word and sets the input data acknowledge line, IN DATA ACK. With this line set, IDA goes high. INPS and IDA cause clear status signal $\overline{\text{CLRSTAT}}$ (Sheet 22) to go low. The low $\overline{\text{CLRSTAT}}$ signal resets RJT and causes INPS to go false. With RJT and INPS both false, EF also goes false. INPS going false also removes $\overline{\text{EIR}}$, Sheet 21, and the MTS is ready for a new command.

3.8.2 Write One Record

The write command code is 0001. This command causes an erasure of specified length on tape to provide an inter-record gap. The standard gap length is 0.6 inch for 9-track tape, 0.75 inch for 7-track tape and 3.75 inches if EIRG is set. The output data request line (ODR) is then set to request the first 16-bit data word. The word is written on tape in a format corresponding to whether 7-track or 9-track recording is being used. The ODR line is again set to request the next 16-bit word. This process is repeated until the Computer does not return an output data acknowledge signal (ODA) in response to ODR.

If the Computer fails to acknowledge an ODR signal by the time the data is needed, data transfer stops and the write operation is terminated.

When the last data word has been written, the tape stops, the status word is placed on the ID lines and EXT INT REQ is set to signal completion of the operation.

Parity checks are performed by the formatter read-after-write circuitry and, therefore, the program can check the status word for the presence of a parity error.

The logic sequence up to and including the loading of the command register, is identical to that explained in the NO operation discussion. In this case, however, the low-active output from the 4-to-10 line decoder is $\overline{WT}$.

The low $\overline{WT}$ signal is applied to inverter D11-4 to provide a high WT output. This signal enables NAND-Gates B5-8 and B5-3. Whether 7-track write ($\overline{7TW}$) or 9-track write ($\overline{9TW}$) goes low is dependent upon the $\overline{E7TRK}$ and $\overline{E9TRK}$ signals from Sheet 6 of the logic. The low $\overline{WT}$ signal disables NAND-Gate L5-8 on Sheet 11 and, therefore, RSET can be generated only by the output of NAND-Gate A8-3 when the write/read flip-flop (WRTE/READ) is set and the selected unit is file protected (FPRO).

The high WT signal enables the WRTE/READ flip-flop (Sheet 8) to be clocked set by start clock (SCLK). With WRTE high, inverter D15-10 provides the external write signal ($\overline{EWRTE}$) to the formatter. Generation of SCLK is initiated when the LEG flip-flop is clocked set by $\overline{EFAT}$ (Sheet 11). Since $\overline{NOOP}$ and the invalid signal ($\overline{INV}$) are both high, LEGL goes low, indicating that the command is legal.

Refer to Sheet 12. Approximately 270 nanoseconds after $\overline{LEGL}$ goes low, the output of inverter B2-10 goes high. Since LEGL is again high at this time, a negative-going pulse occurs at the output of NAND-Gate A2-8. Approximately 270 nanoseconds later, the output of inverter B2-6 goes high, providing a positive-going SCLK pulse out of inverter C2-4. The negative-going edge of this pulse sets the WRTE-READ flip-flop and, in conjunction with $\overline{RJT}$, trgigers a one-shot (Sheet 12) that provides the execute pulse ($\overline{ESETX}$) to the formatter. Note that the set synchronous forward order ($\overline{ESSFC}$) to the formatter (Sheet 8) is true (low) except when one of the reverse modes of operation is selected. However, the tape is not started until $\overline{ESETX}$ is given.

The WRTE, data buffer not full ($\overline{DBFL}$), down ramp not starting ($\overline{REND}$)

signal and the output data acknowledge not signal ($\overline{ODA}$) cause the output of NAND-Gate E4-6 ($\overline{ODR}$, Sheet 9) to go low. The low ODR signal sets the OUT DATA REQ line (Sheet 4).

The Computer then places data on the OD lines and sets the OUT DATA ACK line. This forces $\overline{ODA}$ low which, in turn, removes ODR. The low $\overline{ODA}$ signal provides a high output enable signal (OTEN, Sheet 17) which enables the NAND-Gates in the data register (Sheets 15, 16 and 17) that have the data signals from the Computer (CIDOO through CID15) as their other inputs. When the output data clock (ODCLK) goes high (approximately 270 nanoseconds after $\overline{ODA}$ goes low), the outputs of the NAND-Gates are loaded into the data register flip-flops. WRTE and the $\overline{Q}$ output of the data buffer full flip-flop (DBFL) enable DBFL to set on the trailing edge of ODCLK. The leading edge of ODCLK resets the pack/unpack counter flip-flops A and B (Sheet 21).

When the formatter issues the buffer ready signal ($\overline{EBUFR}$, Sheet 19), BUFR goes high. This causes flip-flop H2 on Sheet 9 to set. The Q output of the flip-flop is AND'ed with WRTE to provide the output exchange signal ($\overline{EOUTX}$) to the formatter.

Refer to Sheets 20 and 21. Sheet 20 shows the pack/unpack logic; Sheet 21 shows the byte counter flip-flops (A and B). Seven-track write operations are accomplished in three bytes. Nine-track operations are accomplished in two bytes.

3.8.2.1 Seven-Track Write

Assuming that a 7-track unit has been selected, signals $\overline{E7TRK}$ and $\overline{7TW}$ on Sheet 20 are both low. The counter flip-flops on Sheet 21 have been previously reset by ODCLK. Under these conditions, signal 70BT1 is high and is applied to NAND-Gates C14-11, C13-11, C12-11 and B14-11 in the output data gating logic on Sheets 13 and 14. The other inputs to these

gates are DB12 through DB15 from the data register. Thus, the four most significant bits are put on the output line to the formatter.

When BUFR goes negative, flip-flop A is set and B remains reset, thereby causing the output of AND-Gate E5-8 (70BT2, Sheet 20) to go high. This signal enables NAND-Gates C14-6, C13-6, C12-6, B14-6, B13-6 and B12-6- putting the second byte, DB06 through DB11 on the output lines to the formatter.

The next negative-going transition of the BUFR signal resets flip-flop A and sets B. In this condition, signal 7/90UT goes high, enabling NAND-Gates C14-8, C13-8, C12-8, B14-8, B13-8 and B12-8, putting the third byte, DB00 through DB05 on the output lines.

When 7/90UT goes high, the clock input to the DBL flip-flop on Sheet 10 also goes high. The next BUFR signal clocks flip-flop A set, thereby causing 7/90UT to go false, resetting DBFL. The $\overline{\text{ODR}}$ signal again goes low, indicating to the Computer that the MTS is ready for another data word.

3.8.2.2 Nine-Track Write

Writing in the 9-track format is similar to that of the 7-track format except that the data word is transferred in two bytes.

With flip-flops A and B reset and $\overline{\text{9TW}}$ low, the output of AND-Gate D5-8 (90BT1, Sheet 20) goes high. This signal enables the NAND-Gates that have the most-significant half of the data word (DB08 through DB15, Sheets 13 and 14) as their data inputs. When BUFR goes low, flip-flop A is set and B remains reset. $\bar{A}$, B and $\overline{\text{9TW}}$ cause the output of AND-Gate C5-8 (90BT2) to go high. The 90BT2 signal is applied to NOR-Gate J5-3, producing a high 7/90UT signal at the output of inverter K6-2.

The 90BT2 and 7/90UT signals enable the NAND-Gates that have the least-significant half of the data word (DB00 through DB07) as their data inputs.

3.8.2.3 Write Termination

The write operation is terminated when the Computer fails to respond to an $\overline{\text{ODR}}$ signal with and $\overline{\text{ODA}}$. The formatter then writes the LRCC and/or CRCC and issues a device stop order pulse ($\overline{\text{EDSTP}}$, Sheet 19). The low $\overline{\text{EDSTP}}$ signal generates a high DSTP signal and its complement. The down ramp starting flip-flop (REND, Sheet 22) is clocked set by the negative-going transition at the output of inverter J1-12 when $\overline{\text{DSTP}}$ returns high. The low $\overline{\text{REND}}$ signal removes $\overline{\text{ODR}}$ (Sheet 9). The inverter also provides RCLK which sets the busy flip-flop (BSY). Terms BSY, $\overline{\text{INPD}}$ and TPCR cause the output of NAND-Gate L2-8 to go low, providing a high INSP signal at the output of OR-Gate K3-6. The status word is then put on the ID lines. $\overline{\text{INPD}}$ and INPS generate $\overline{\text{EIR}}$ which sets the EXT INT REQ line. The Computer reads the status word and responds with IDA. The INPS and IDA cause clear status signal $\overline{\text{CLRSTAT}}$ (Sheet 22) to go low, thereby resetting BSY which, in turn, causes INSP to go false. INSP going false removes $\overline{\text{EIR}}$ and the MTS is ready for a new command.

3.8.2.4 Extended Inter-Record Gap

Setting bit CID06 causes a 3.75-inch erasure to occur on the tape. This feature is used in conjunction with the write command to automatically provide an extended inter-record gap (EIRG) prior to command execution.

Refer to Sheet 5. When used in conjunction with the write command, the output of inverter D11-4 and EIRG cause the output of NAND-Gate A12-6 ($\overline{\text{EEIRG}}$) to go low. This notifies the formatter that 3.75 inches of tape are to be erased prior to execution of the command. The remaining logic functions are identical to those of the write command.

3.8.2.5 Write File Mark

This command initiates a 3.75-inch erasure on tape, followed by the writing of the file mark code. The tape then stops and the status word is placed on the ID lines. The EXT INT REQ line is set to signal completion of the operation.

The low $\overline{\text{WFM}}$ out of the decoder causes the output of inverter D11-2 (WFM) to go high. The $\overline{\text{WFM}}$ signal also disables the normal reset logic on Sheet 11, indicating that it is a valid command. WFM enables the WRTE/READ flip-flop to set and also provides the external set write file mark order ($\overline{\text{ESWFM}}$, Sheet 8) to the formatter. In addition, WFM pulls BUFR, Sheet 19, low. The remaining logic functions are similar to those of the write command except that the OUT DATA REQ signal from the MTS is not acknowledged and the operation is terminated.

The status word is put on the ID lines and the EXT INT REQ line is set to indicate termination of the operation.

3.8.3 Read One Record

This command causes the tape unit to start the tape in the forward direction. The first three characters in the case of 7-track operation or the first two characters in the case of 9-track operation, are a assembled in the MTS storage register and placed on the ID lines. The IN DATA REQ line is then set to indicate that data is available on the ID lines. The Computer responds by setting the IN DATA ACK line to indicate that it has sampled the data. The IN DATA REQ line is then reset. This process is repeated until the entire record has been read.

If the Computer fails to respond by the time that the next data word has been read into the storage register, the data transfer is terminated.

When the last word in the record has been read, tape motion is stopped, the status word is placed on the ID lines, and the EXT INT REQ line is set to indicate completion of the operation.

The logic sequence up to, and including, the loading of the command register is identical to that explained in the NO operation discussion. In this case, however, the low-active output from the 4-to-10 line decoder is $\overline{RD}$.

Refer to Sheet 5. The low $\overline{RD}$ signal is applied to inverter C11-6. The high output of the inverter enables NAND-Gates B5-6 and B5-11. Whether 7-track read ($\overline{7TR}$) or 9-track read ($\overline{9TR}$) goes low is dependent upon the $\overline{E7TRK}$ and $\overline{E9TRK}$ signals from Sheet 6 of the logic. The low RD signal also disables the normal RSET logic on Sheet 11.

The low WT signal enables the WRTE/READ flip-flop to reset on the SCLK pulse, the generation of which has been discussed previously. The high Q output of the flip-flop provides a high READ signal and is also inverted to supply a low external read command ($\overline{EREAD}$) to the formatter.

The $\overline{ESETX}$ pulse causes the formatter to begin the read sequence. When the formatter is ready to begin data transfer, it provides a low $\overline{EBUFR}$ signal (Sheet 19) which causes BUFR to go high. BUFR, READ and $\overline{DBFL}$ (Sheet 9) force the output of NAND-Gate A3-6 low, clocking flip-flop H2 set. The high Q output of flip-flop H2 and READ provide two 270-nanosecond clock pulses. One is the external input exchange pulse to the formatter ($\overline{EINPX}$); the other is the data register clock, INCLK.

Upon receipt of $\overline{EINPX}$, the formatter gates the first character onto the input data lines to the interface ($\overline{ID00}$ through ID07, Sheet 18). These inputs are inverted and designated RB00 through RB07, respectively. These signals are applied to the data register logic shown on Sheets 15, 16 and 17. Entry of data into the register latches is controlled by the pack/unpack counter and control logic.

3.8.3.1 Seven-Track Read

Assuming that a 7-track unit has been selected, signals $\overline{\text{E7TRK}}$ and $\overline{\text{7TR}}$ on Sheet 20, are both low. With counter flip-flops A and B on Sheet 21 both reset, signal 7BT1 on Sheet 20 is high. This signal enables the NAND-Gates on Sheet 17 that have RB00 through RB03 as their data inputs. The complements of the outputs of the NAND-Gates are transferred to the $\overline{\text{Q}}$ outputs of their respective latches when CLK4 is high. CLK4 is provided by INCLK and 7BT1 (Sheet 21). When INCLK goes low, the data is latched.

When BUFR goes low, counter flip-flop A is set and B remains reset. When BUFR goes high, $\overline{\text{EINPX}}$ and INCLK are again generated and the formatter puts the next character on the lines. At this time, 7BT2 (Sheet 20) is high. The 7BT2 signal enables the gates with RB00, RB01 (Sheet 15) and RB02 through RB05 (Sheet 16) as their data inputs. The data is transferred to the latches on Sheet 15 by INCLK and ENCLK7-6, which is derived from 7BT2 (Sheet 20). When INCLK goes low, the data is latched. The data on Sheet 16 is transferred to the latches by INCLK and 7BT2.

The last byte is enabled by 7/9BT (Sheet 15) and latched when INCLK goes low. The latch outputs (DB00 through DB15) are sent to NAND-Gates on Sheets 23 and 24. The enabling signal to these gates is input data (INPD) which is generated on Sheet 10.

READ, $\overline{\text{DBFL}}$, and 7/9BT cause the output of NAND Gate H3-8 to go low. The output of OR-Gate K3-8 then goes high. When 7/9BT goes low, indicating that the last character is latched, the output of the OR-Gate also goes low, clocking DBFL set. DBFL generates a 130 nanosecond leading edge pulse (EDBFL, Sheet 9). READ, $\overline{\text{INPD}}$ and EDBFL cause the output of NAND-Gate K1-12 (Sheet 10) to go low, setting the INPD flip-flop.

The high INPD signal enables the NAND-Gates on Sheets 23 and 24 to supply their outputs (COD00 through COD15) to the line drivers on Sheets 25 through 27. The line drivers put the data on the ID lines ($\overline{\text{IDB00}}$ through $\overline{\text{IDB15}}$). The high INPD signal also resets the counter flip-flops (A and B, Sheet 21).

The low $\overline{\text{INPD}}$ signal in conjunction with the high $\overline{\text{IDA}}$ signal generate a low $\overline{\text{IDR}}$ (Sheet 9). $\overline{\text{IDR}}$ sets the IN DATA REQ line (Sheet 27). The Computer samples the data and then sets IN DATA ACK (Sheet 27) causing IDA to go high. The low $\overline{\text{IDA}}$ signal removes $\overline{\text{IDR}}$. The high IDA, READ and INPD signals cause the output of NAND-Gate K1-8 to go low, resetting INPD, which also causes DBFL to reset. The MTS is then ready for the next character. This process is repeated until the last character in the record has been read.

3.8.3.2 Nine-Track Read

Reading in 9-track format is similar to that of 7-track format except that the data word is transferred in two bytes.

With flip-flops A and B reset and $\overline{\text{9TR}}$ low, the output of AND-Gate C5-6 (9BT1, Sheet 20) goes high. This signal enables the NAND-Gates that have the first (most-significant) half of the data word as their data inputs (Sheets 16 and 17). When BUFR goes low, A is set and B remains reset. $\overline{\text{A}}$, B and $\overline{\text{9TR}}$ being low cause the output of AND-Gate E5-8 (9BT2) and to go high. This signal produces 7/9BT. Both signals are used to enable the NAND-Gates that have the least-significant half of the data word as their data inputs (Sheet 15).

3.8.3.3 Read Termination

The read operation is terminated by the formatter when the inter-record gap is detected. When the formatter detects the gap, it sends the $\overline{\text{EDSTP}}$

pulse (Sheet 19) which generates the high DSTP signal and its complement. The REND flip-flop (Sheet 22) is clocked set by the negative-going transition at the output of inverter J1-12 when $\overline{\text{DSTP}}$ returns high. The REND signal causes the output of NOR-Gate K4-8 (Sheet 10) to go low, resetting INPD. The high $\overline{\text{INPD}}$ signal removes $\overline{\text{IDR}}$ (Sheet 9).

Inverter J1-12 also provides RCLK which sets BSY. Terms BSY, $\overline{\text{INPD}}$ and TPCR cause the output of NAND-Gate L2-8 to go low, providing a high INPS signal at the output of OR-Gate K3-6. The status word is then put on the ID lines. $\overline{\text{INPD}}$ and INPS generate $\overline{\text{EIR}}$ which sets the EXT INT REQ line. The Computer reads the status word and responds with IDA. The INPS and IDA signals cause $\overline{\text{CLRSTAT}}$ (Sheet 22) to go low, thereby resetting BSY which, in turn, causes INPS to go false. INPS going false removes $\overline{\text{EIR}}$ and the MTS is ready for a new command.

3.8.4 Space Forward One Record

This command initiates forward tape motion until the end-of-tape, end-of-record or file mark is detected, at which time tape motion is stopped. The status word is then placed on the ID lines and EXT INT REQ is set to indicate completion of the operation.

Refer to Sheet 5. When the space forward one record command is issued, the low-active output out of the 4-to-10 line decoder is $\overline{\text{SPFR}}$. This signal causes the outputs of inverter C11-4 (SPFR) and J3-8 (SPCO) on Sheet 5 to go high. $\overline{\text{SPFR}}$ is also used to inhibit the normal RSET command on Sheet 11.

SPFR is applied to NAND-Gate A8-6, on Sheet 11, to generate RSET if the end-of-tape signal (EOT) is high.

SPCO (space command) is used on Sheet 11 to hold INPD reset and on Sheet 21 to hold flip-flops A and B reset. The remaining logic functions are similar to those explained for the read command except that no data is exchanged because INPD is held false. This also disables $\overline{IDR}$.

When the end-of-tape, file mark or end-of-record is detected, the formatter issues the $\overline{EDSTP}$ pulse and the operation is terminated in the same manner as for the read operation.

3.8.5 Space Reverse One Record

This command initiates reverse tape motion. It is similar to space forward except that the beginning-of-tape marker (BOT) replaces EOT as one of the terminating conditions.

Refer to Sheet 5. When the space reverse command is given, the low-active output out of the 4-to-10 line decoder is $\overline{SPRV}$. This signal causes the outputs of inverters C11-2 (SPRV) and J3-8 (SPCO) to go high. The low $\overline{SPRV}$ signal inhibits the normal RSET logic on Sheet 11.

SPRV is applied to NOR-Gate C10-6 on Sheet 8. This causes the external set synchronous forward command ($\overline{ESSFC}$) to the formatter to go false and the external set synchronous reverse command ($\overline{ESSRC}$) to go true. SPRV is also used on Sheet 11 to generate RSET if BOT is true.

SPCO is used as explained previously. When one of the three conditions is met, the operation is terminated.

3.8.6 Set File Search Forward

This command initiates forward motion of the tape until a file mark is detected. Tape motion does not terminate at EOT, thereby allowing the user to close out files after detecting EOT.

When the command is given, the low-active output out of the 4-to-10 line decoder is $\overline{SFSF}$. This signal is used on Sheet 8 to generate the external set file search forward command ($\overline{ESFSF}$) command to the formatter. It is also used on Sheet 11 to inhibit the normal RSET logic.

The logic functions involved are similar to read except that the Computer does not respond to IN DATA REQ and, therefore, no data is transferred. When a file mark is detected, the operation is terminated in the same manner as for the read operation.

3.8.7 Set File Search Reverse

This command initiates reverse tape motion. Otherwise, it is similar to set file search forward except that tape motion will stop at BOT if a file mark is not detected.

Refer to Sheet 5. When this command is given, the low-active output out of the 4-to-10 line decoder is SFSR. This signal is used on Sheet 8 of the logic where it causes the external file search reverse ($\overline{ESFSR}$) and external set synchronous reverse ($\overline{ESSRC}$) commands to go low, and the external set synchronous forward command (ESSFC) to go high. It also provides a high SFSR at the output of inverter D11-12. $\overline{SFSR}$ is used on Sheet 11 to inhibit the normal RSET. SFSR is used on Sheet 11 to generate RSET if BOT is high.

Termination of the operation occurs when either a file mark or BOT is detected.

3.8.8 Rewind

This command causes the tape to rewind to the load point. The status word is then put on the ID line and EXT INT REQ is set to signal completion upon receipt of $\overline{ERWIG}$ from the formatter.

A different tape unit can be selected immediately after the rewind command is given and EXT INT REQ is received and honored. This is the only time that a select command can be issued while the controller is busy. The new command to the selected tape deck is handled in the normal manner. Refer to Sheet 5. When the rewind command is given, the low-active output out of the 4-to-10 line decoder is $\overline{\text{RWND}}$. This signal is used on Sheet 5 to provide a high RWND. It is also used on Sheet 12 to disable $\overline{\text{ESETX}}$ to the formatter. The $\overline{\text{ESETX}}$ signal is disabled because the only action required by the formatter is to relay the rewind command to the tape drive and to return a rewinding status signal from the drive to the interface.

RWND is used as the set enable input for flip-flop B10 on Sheet 8. The flip-flop is clocked set by the trailing edge of SCLK when RWND is high. The high Q output of the flip-flop is applied to NAND-Gate B16-3. The other input into this NAND-Gate is CCLK which is derived from the formatter quarter character clock ($\overline{\text{C}}$, Sheet 18). When CCLK goes high, the external rewind command ($\overline{\text{ERWD}}$) goes low.

The high RWIG signal causes the output of inverter A11-2 (Sheet 8) to go low, resetting flip-flop B10. The high RWIG signal also enables the CMDCLK logic (Sheet 7) so that another tape transport can be selected immediately.

The high RWND signal is also used on Sheet 11 to generate RSET in the event that BOT is high (NAND-Gate A3-12). In addition, RWND is applied to NAND-Gate K1-6, Sheet 22. The other inputs into this gate are RWIG and the output of inverter L1-6, which is normally high. When RWIG goes high, the output of the NAND-Gate goes low and the clock input into flip-flop K2 goes high. At the end of the propagation delay time through inverters L1-2, L1-4 and L1-6 (approximately 140 nanoseconds max.), the output of the NAND-Gate returns high and a negative-going transition occurs at the clock input of flip-flop K2, clocking it set.

The low $\overline{Q}$ output of the flip-flop causes INPS to go high and the status word is put on the ID lines. The EXT INT REQ line is then set.

3.8.9 Invalid Command

When the four low-order bits of the function command are greater than "1000", an invalid condition exists. The low-active signal out of the decoder is $\overline{INV}$. This signal is sent to NAND-Gate B3-3 on Sheet 11. The logic sequence involved is identical to the NO operation sequence.

3.8.10 Master Clear

Setting bit CID04 causes the interface and formatter logic to be initialized. Refer to Sheet 9. Bit CID04 is applied, along with EFA, to the input of NAND-Gate E3-8. When the output of the NAND-Gate goes low, the output of OR-Gate E3-6 (PUP) goes high. At the same time, the output of NAND-Gate H1-6 ($\overline{PUP}$) goes low. These signals are also supplied on initial power turn-on through the resistive-capacitive circuit at the other input of OR-Gate E3-6.

PUP is used to generate $\overline{CLR}$ on Sheet 10 and $\overline{EINZT}$ on Sheet 12. PUP, $\overline{PUP}$, $\overline{CLR}$ and $\overline{EINZT}$ are used throughout the interface logic for initialization. $\overline{EINZT}$ is also sent to the formatter.

3.8.11 Overwrite

Setting bit CID05 along with the write command enables an edit operation to be performed.

Refer to Sheet 8. BIT CID05 is the set enable input into flip-flop B11. If CID05 is high, the flip-flop sets on the negative-going edge of STCLK. The high Q output is applied to the input of NAND-Gate A12-8,

along with WRTE. The output of the NAND-Gate is the external edit command (EEDIT) to the formatter. The combination of $\overline{\text{EEDIT}}$ and $\overline{\text{EWRTE}}$ being low enables writing over previously written portions of the tape.

3.9 EXTERNAL FORMATTER SELECT SIGNAL

The external formatter select signal ($\overline{\text{EFMTS}}$) is shown at the bottom of Sheet 8. This signal is held at ground and, therefore, the formatter is always selected.

3.10 DENSITIES AVAILABLE

The densities available signal (8/2) is shown at the bottom of Sheet 8. This signal is used in conjunction with $\overline{\text{LODN}}$ and $\overline{\text{8HI}}$ to indicate to the formatter what densities are available in 7-track operation. In this application, the signal is held at ground, indicating that the two densities available are other than 800 and 200 BPI.

3.11 ODD CHARACTER DETECT

The odd character detect flip-flop is shown on Sheet 21. The purpose of this flip-flop is to provide an indication to the Computer when an odd number of characters has been read in the last record. The program should then "strip off" the even characters of the last word since it is meaningless.

The flip-flop is enabled to be clocked set by DSTP when either flip-flop A or B is set, or when $\overline{\text{7/9BT}}$ is low. The high ODDC signal is sent to Sheet 24 and is put on the ID lines when INPS goes high.

SECTION IV
MAINTENANCE AND TROUBLESHOOTING

4.1 GENERAL

Maintenance is generally divided into two categories, preventive and corrective maintenance. Preventive maintenance consists of periodic checks, performance of diagnostics and other precautionary steps which may be taken to prevent malfunctions. Corrective maintenance takes place after a malfunction occurs and consists of locating and correcting the fault.

Because of the non-mechanical nature of the MTS there is little to be done in the way of preventive maintenance. Periodic checking of dc voltages, tightness of mating connectors and weekly performance of the diagnostic will suffice for the MTS. If any discrepancies appear, they should be corrected at this point.

The tape transport manufacturer's maintenance instructions should be followed closely with particular attention being paid to the requirement for tape head and tape path cleaning.

4.2 TROUBLESHOOTING

When the magnetic tape subsystem fails to perform correctly, it is wise to begin the troubleshooting process with the formatter since it is central to all processes in the system. Troubleshooting procedures for the formatter are provided in the formatter manual. The procedures used for the 1616 Interface are essentially the same.

It is recommended that a functional analysis approach be used in locating the cause of an operational discrepancy. This is, the fault can generally be traced to a functional area such as receiver circuits, transmitter

circuits, command and control circuits, etc., and detailed analysis can then be undertaken. Use of the logic diagrams will aid in fault analysis and troubleshooting.

To provide a systematic approach to fault analysis and identification, proceed as follows:

1. Inspect the equipment for loose connections, etc.
2. Check power supply operation and voltages.
3. Perform system functional checks.

Table 4-1 is a troubleshooting guide.

Generally, most maintenance and troubleshooting can be performed without removing the formatter PCB or the Interface PCB from the chassis. If, however, removal does become necessary, proceed as follows:

WARNING

Prior to beginning this procedure, insure that power to the processor, tape units and formatter is off to avoid injury to personnel and/or damage to equipment.

1. Disconnect processor cables at formatter rear panel.
2. Disconnect tape drive connectors at formatter near panel.
3. Remove the Phillips-head screws from the COMPUTER IN 1 and COMPUTER OUT 1 connectors on the rear panel.
4. Remove the five Phillips-head screws holding the rear panel to the chassis.
5. The rear panel may now be placed across the top of the chassis to gain access to the PCB. Use caution to avoid putting strain on the AC input connection.
6. Remove the PCB by pulling it straight back.
7. To reinstall, reverse the above steps.

Table 4-1

Troubleshooting Guide

Symptom	Probable Cause	Remedy
No response to CPU commands and no interrupt returned	a. I/O cables reversed. b. No -12 Volts to interface. c. IOC incompatible with controller configuration. (i.e., -3 Volt IOC; +3.5 Volt controller.	a. Install cables properly b. Install -12 Volt jumper correctly (XP3) c. Change to appropriate type IOC or consult factory for controller modification.

4.3 INTERFACE PCB TEST POINTS

Test points are provided on the top of the Interface PCB and are clearly marked. This enables the user to access the test points from the top by removing the cover. Table 4-2 lists the Interface PCB test points and references the applicable timing diagram(s).

Table 4-2

Interface PCB Test Points

Test Point	Timing Diagram
A	Figures 4-4, 4-5
B	Figures 4-4, 4-5
BUFR	Figures 4-4, 4-5
CMDCLK	Figures 4-1, 4-3
DBFL	Figures 4-4, 4-5
EFA	Figures 4-1, 4-2, 4-4, 4-5
$\overline{\text{EINPX}}$	Figure 4-4
$\overline{\text{EIR}}$	Figure 4-5
$\overline{\text{EOUTX}}$	Figure 4-5
$\overline{\text{IDR}}$	Figure 4-4
INPD	Figure 4-4
INPS	Figure 4-5
ODA	Figure 4-5
ODCLK	Figure 4-5
$\overline{\text{ODR}}$	Figure 4-5
RD	Figure 4-3
RD STAT	Figure 4-2
RWND	Figure 4-3
SETX	Figures 4-4, 4-5
SFSF	Figure 4-3
SFSR	Figure 4-3
SPFR	Figure 4-3
SPRV	Figure 4-3
TPCR	Figures 4-1, 4-5
WFM	Figure 4-3
WRTE	Figure 4-5
WT	Figure 4-3

SECTION V
MNEMONIC LIST

5.1 MNEMONICS

This section contains a listing, definitions and origins of the mnemonics used in the logic diagrams. Refer to Table 5-1.

Table 5-1
Mnemonic List

Mnemonic	Origin	Meaning
A	21	Count of One, Pack/Unpack Counter
B	21	Count of Two, Pack/Unpack Counter
BOT	19	Begining-of-Tape
BSY	22	Controller Busy
BT	19	Bad Tape (Status Bit)
BUFR	19	Formatter Buffer Ready for Transfer
$\overline{C}$	18	Quarter-Character Clock Complement
CCLK	18	Quarter-Character Clock
CID00-CID05	1	Computer Input Data Bits 00 (LSB) through 05
CID06-CID11	2	Computer Input Data Bits 06 through 11
CID12-CID15	3	Computer Input Data Bits 12 through 15 (MSB)
CLK	7	Ready Clock
CLK4	21	Data Buffer Clock, Most-Significant Four Bits
CLK6LB	15	Data Buffer Clock, Least-Significant Six Bits

Table 5-1 (Cont'd)

Mnemonic List

Mnemonic	Origin	Meaning
CLK6-7	15	Data Buffer Clock, Bits Six and Seven
$\overline{\text{CLOCK}}$	7	Parameter Clock Complement
CLR	10	Clear
$\overline{\text{CLRSTAT}}$	22	Clear Status
CMDCLK	7	Command Clock
$\overline{\text{COD00}}$-$\overline{\text{COD06}}$	23	Computer Output Data Bits 00 (LSB) through 06
$\overline{\text{COD07}}$-$\overline{\text{COD15}}$	24	Computer Output Data Bits 07 through 15 (MSB)
DB00-DB07	15	Data Bits 00 (LSB) through 07
DB08-DB11	16	Data Bits 08 through 11
DB12-DB15	17	Data Bits 12 through 15 (MSB)
DBFL	10	Data Buffer Full
DSTP	19	Device Stop Order
$\overline{\text{EBOT}}$	19	External Beginning-of-Tape
$\overline{\text{EBUFR}}$	19	External Buffer Ready
$\overline{\text{EDBFL}}$	9	Leading-Edge Pulse, Data Buffer Full
$\overline{\text{EDOB0}}$-$\overline{\text{EDOB2}}$	14	Data Output to Formatter
$\overline{\text{EDOB3}}$-$\overline{\text{EDOB7}}$	13	Data Output to Formatter (EDOB7 is MSB)
$\overline{\text{EDSTP}}$	19	Device Stop Order from Formatter
$\overline{\text{EEDIT}}$	8	External Edit Command
$\overline{\text{EEIRG}}$	5	External Write with Extended Inter-Record Gap

Table 5-1 (Cont'd)

Mnemonic List

Mnemonic	Origin	Meaning
$\overline{\text{EEOF}}$	19	External End-of-File
$\overline{\text{EEOT}}$	19	External End-of-Tape
$\overline{\text{EERASE}}$	5	External Erase
EF	7	Error Flag
EFA	4	External Function Acknowledge
EFAT	11	Trailing Edge Pulse, External Function Acknowledge
$\overline{\text{EFMTS}}$	8	External Formatter Select
EFPRO	18	External File Protect
EINPX	9	Input Data Clock, Interface to Formatter
EINZT	12	Initialize Pulse, Interface to Formatter
$\overline{\text{EIR}}$	21	External Interrupt Request Complement
EIRG	5	Extended Inter-Record Gap
ENCLK7-6	20	Enable Bits 6 and 7 Clock
EOF	19	End-of-File
EOT	19	End-of-Tape
EOUTX	9	Output Exchange Pulse to Formatter
EPERE	19	External Redundancy Error
EREAD	8	External Read Mode Order to Formatter
ERWD	8	External Rewind Order to Formatter
ERWIG	18	Rewinding Status Signal rom Formatter
ESE01-ESE04	6	Tape Drive Select to Formatter

Table 5-1 (Cont'd)

Mnemonic List

Mnemonic	Origin	Meaning
ESETX	12	Execute Pulse to Formatter
ESFSF	8	Set File Search Forward Order to Formatter
ESSFC	8	Set Synchronous Forward Order to Formatter
ESSRC	8	Set Synchronous Reverse Order to Formatter
ESWFM	8	Set Write File Mark Order to Formatter
ETGAP	19	External Tape Gap Signal
ETPCR	19	External Tape Ready Signal
EWRTE	8	External Write Mode Order to Formatter
EXT FUNC ACK	4	External Function Acknowledge
EXT FUNC REQ	4	External Function Request
EXT INT REQ	27	External Interrupt Request
E7TRK	6	7-Track Select
E9TRK	6	9-Track Select
FPRO	18	Selected Tape Drive File Protected
IDO0-IDO3	5	Input Data Bits 00 through 03
IDO0-IDO7	18	Input Data Bits 00 through 07 from Formatter
IDA	27	Input Data Acknowledge
IDB00-IDB06	25	Input Data Bits 00 (LSB) through 06
IDB07-IDB12	26	Input Data Bits 07 through 12
IDB13-IDB15	27	Input Data Bits 13 through 15 (MSB)
IDR	9	Input Data Request Complement

Table 5-1 (Cont'd)
Mnemonic List

Mnemonic	Origin	Meaning
INCLK	9	Data Register Clock, Input Data from Formatter
IN DATA ACK	27	Input Data Acknowledge
IN DATA REQ	27	Input Data Request
INPD	10	Input Data Enable
INPS	22	Input Status Enable
INV	5	Invalid Command Complement
INZT	22	Initialize (Reset) Pulse
INZX	7	Initialize Pre-Command
LEF	4	EFA Leading Edge Pulse
LEG	11	EFAT Trailing Edge Pulse
$\overline{\text{LEGL}}$	11	Legal Command Complement
LODN	6	Low Density Order to Formatter
LTPR	21	Tape Ready Leading Edge Pulse
NOOP	5	NO Operation Command
ODA	4	Output Data Acknowledge Complement
ODB00-ODB05	1	Output Data Bits 00 (LSB) through 05
ODB06-ODB11	2	Output Data Bits 06 through 11
ODB12-ODB15	3	Output Data Bits 12 through 15 (MSB)
ODCLK	4	Output Data Clock
ODDC	21	Odd Character Detect
ODDP	6	Odd Parity

Table 5-1 (Cont'd)

Mnemonic List

Mnemonic	Origin	Meaning
ODR	9	Output Data Request Complement
ONL	23	Tape Unit On-Line Complement
OTEN	17	Output Enable
OUT DAT ACK	4	Output Data Acknowledge
OUT DATA REQ	4	Output Data Request
PERE	19	Parity or Redundancy Error
PUP	9	Power-Up Reset
RB00-RB07	18	Read Bits 00 through 07 (07 is MSB)
RCLK	22	Read Clock
$\overline{RD}$	5	Read Complement
RDSTAT	6	Read Status
READ	8	Read Data Command
REGCLR	7	Clear Command and Select Register
REND	22	Down Ramp Starting
RJT	12	Reject
RSET	11	Reset
RSP	22	Leading Edge Reset Pulse
RWIG	18	Rewinding Status
RWND	5	Rewind Command
SCLK	12	Start Clock
SELPE	6	Select Phase Encode (Dual Deck)
SFSF	5	Start File Search Forward

Table 5-1 (Cont'd)

Mnemonic List

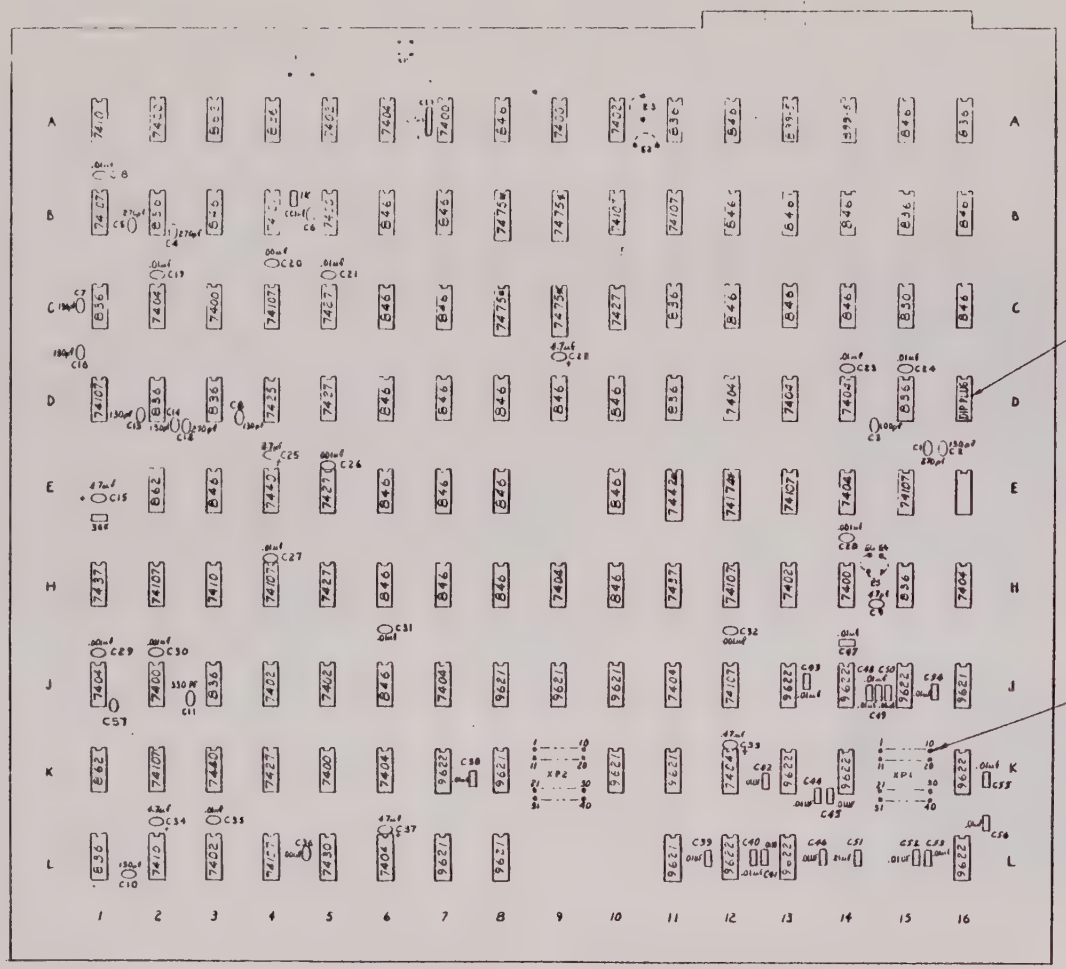
Mnemonic	Origin	Meaning
SFSR	8	Start File Search Reverse
SPFR	5	Space Forward
SPRV	5	Space Reverse
STCLK	7	Delayed Parameter Clock
TGAP	19	Three and One-Quarter Consecutive Characters Missing on Tape
TPCR	19	Tape Drive and Formatter Ready
TPIG	7	Tape Ready or Rewinding
WFM	5	Write File Mark
WRTE	8	Write Command
WT	5	Decoded Write
7BT1	20	7-Track Read Byte One Enable
7BT2	20	7-Track Read Byte Two Enable
7/9BT	20	7 or 9-Track Read Enable
7/9OUT	20	7 or 9-Track Write Enable
7TR	5	7-Track Read
7TW	5	7-Track Write
8/2	8	Densities are 800 and 200 BPI
9BT1	20	9-Track Read Byte One Enable
9BT2	20	9-Track Read Byte Two Enable
9TR	5	9-Track Read
9TW	5	9-Track Write

Table 5-1 (Cont'd)

Mnemonic List

Mnemonic	Origin	Meaning
70BT1	20	7-Track Byte One Out Enable
70BT2	20	7-Track Byte Two Out Enable
90BT1	20	9-Track Byte One Out Enable
90BT2	20	9-Track Byte Two Out Enable

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
F	REVISED PER ECO 4829		
F1	REVISED PER ECO 4829		
G	REV PER ECO 4829		
G1	REVISED PER ECO 4829		
H	REV PER ECO 5321		
J	REV PER ECO 5340		



1 ALL 16 PIN I.C.'s TO BE DENOTED WITH ASTERISK (*).

NOTES: UNLESS OTHERWISE SPECIFIED

UNIVAC MAG TAPE INTERFACE		PPD Datum Inc.	
		D	88003

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
B	REVISED PER ECN 178	4-5-76	J Wuebbeler
C	REVISED PER ECN 208	4-5-76	J Wuebbeler
D	REVISED PER ECN 240	4-5-76	J Wuebbeler
E	REVISED PER ECN 263	4-5-76	J Wuebbeler
F	REVISED & RELEASED PER CO 3352. PRIOR DOC UP TO THIS REVISION LEVEL IS NON-EXISTANT	4-8-76	J Wuebbeler MEB
F_1	REVISED PER ECO 4488	Dwn 12-15-76 M. Eng 12-15-76	MEB 2-17-76
F_2	REVISED PER E.C.O. 4568	LAVELL 1-11-77 M. Eng 1-17	1-21-77
G	REV PER ECO 4829	BC 2-10-78 M Eng 2-16-8	2-17-78
G_1	REVISED PER ECO 5167	db 2-18-78 MV 3-2-78	PM 3 Mar 78
H	REV PER ECO 5321	DD 10/26/78 MV 12-5-78	12-6-78
J	REV PER ECO 5386	DEH 2-14-79 db 2-22-79	PM 23 Feb 79

REF PICO 575118 0

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03 XXX ±.010 ANGLES ±1/2°

TITLE
UNIVAC MAG TAPE INTERFACE

PPD
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

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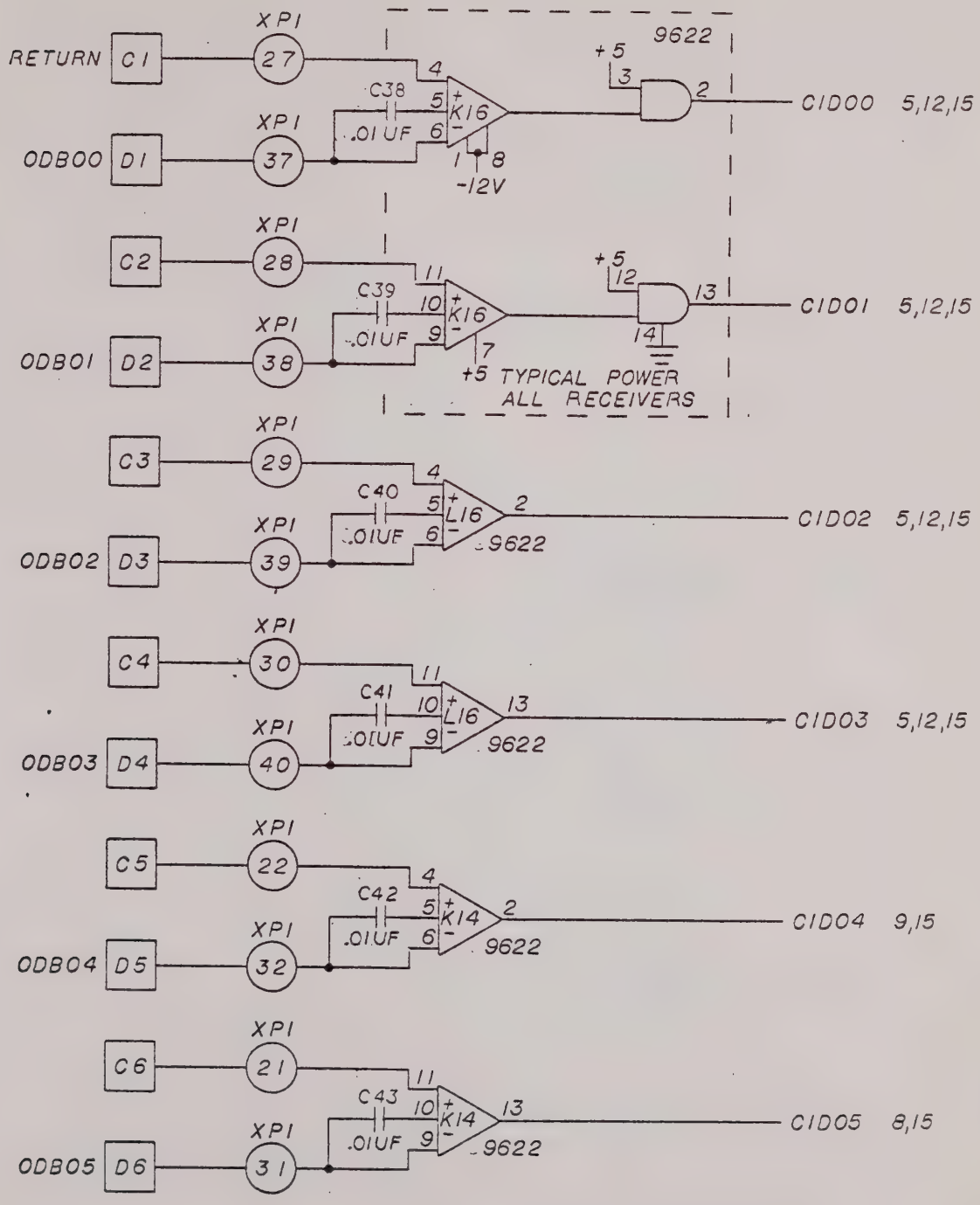
E. GREFE			
CHK		ENGR	
		D. VILLATE	3/7/79

SCALE _____ FSC 31160

SIZE	DWT	REV
B	88003	J

SHT 0 OF 27



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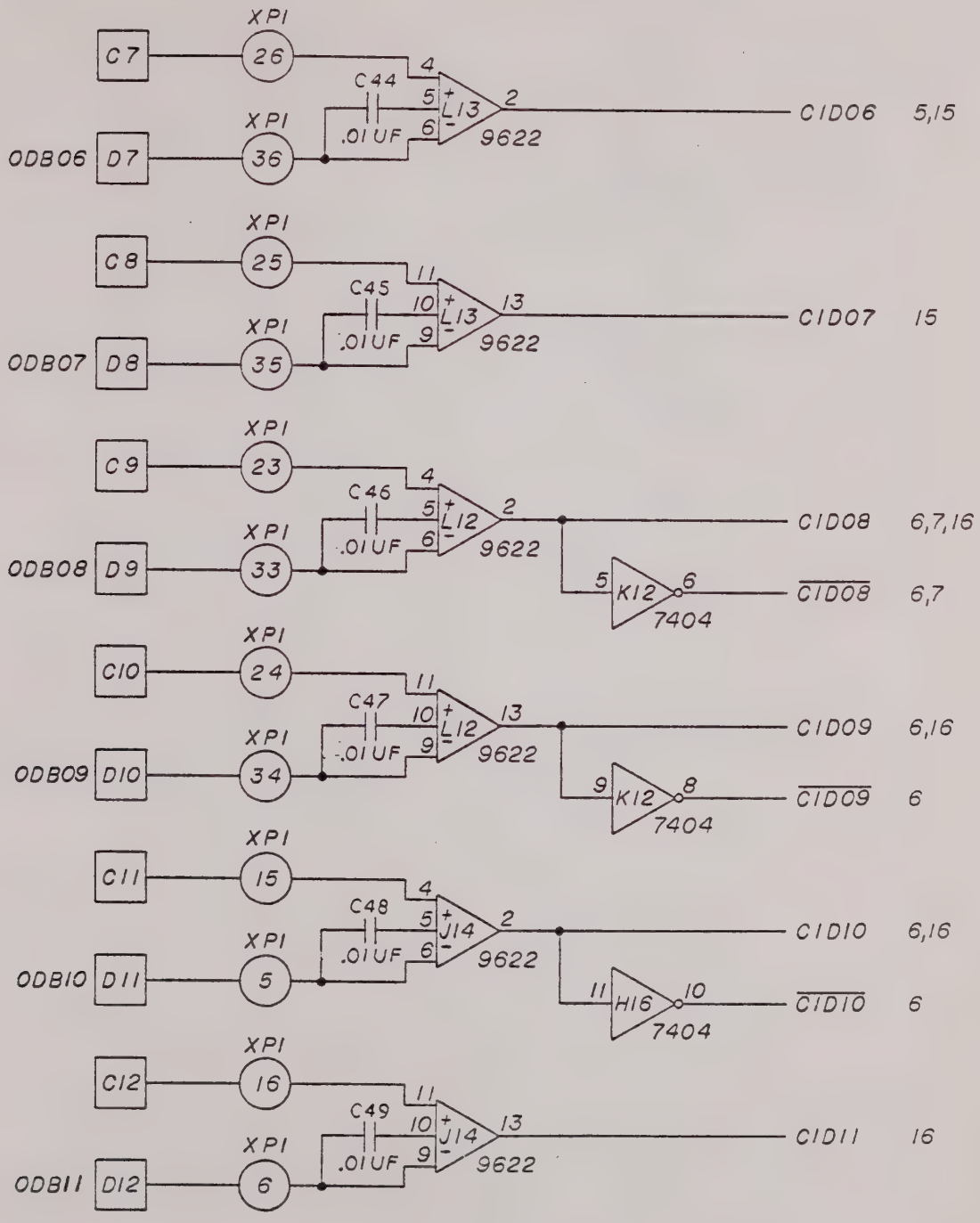
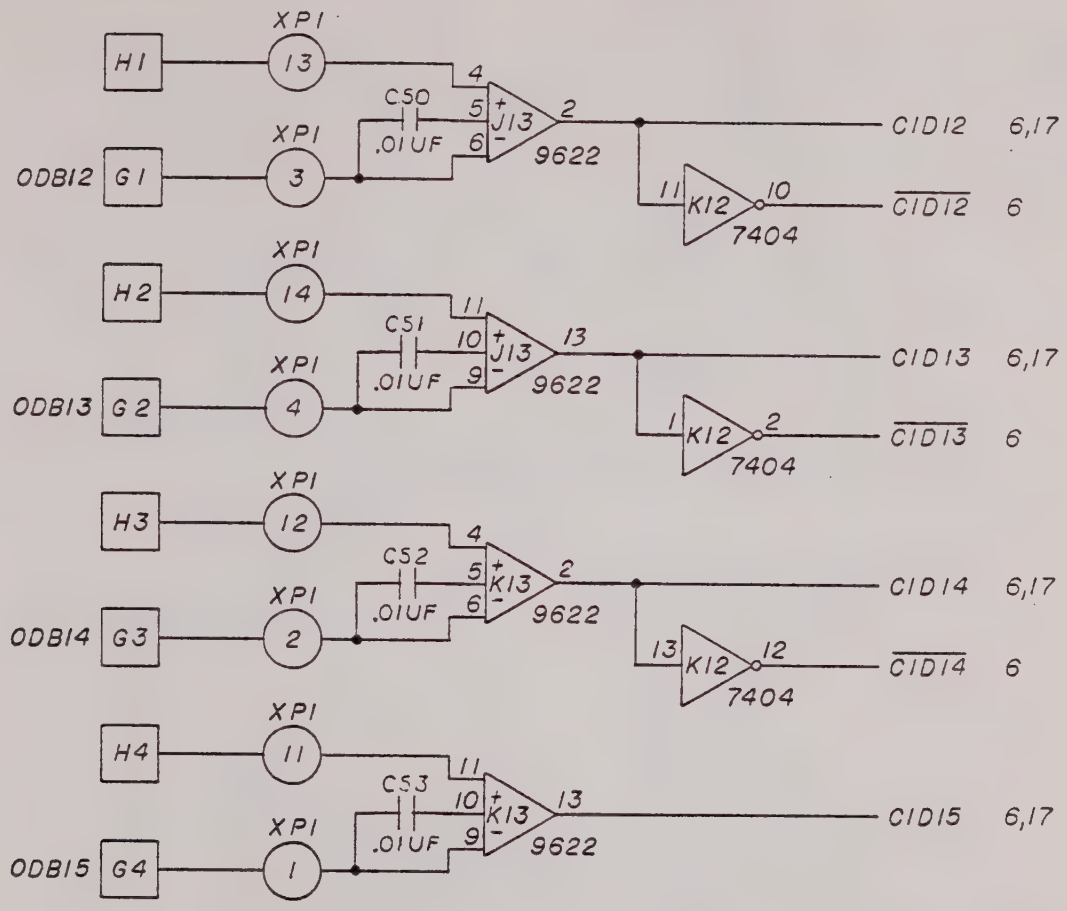


-3V INTERFACE
DATA FROM COMPUTER

REV J
88003 SHEET 2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XP1
H2
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C51
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J13
9622
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XP1
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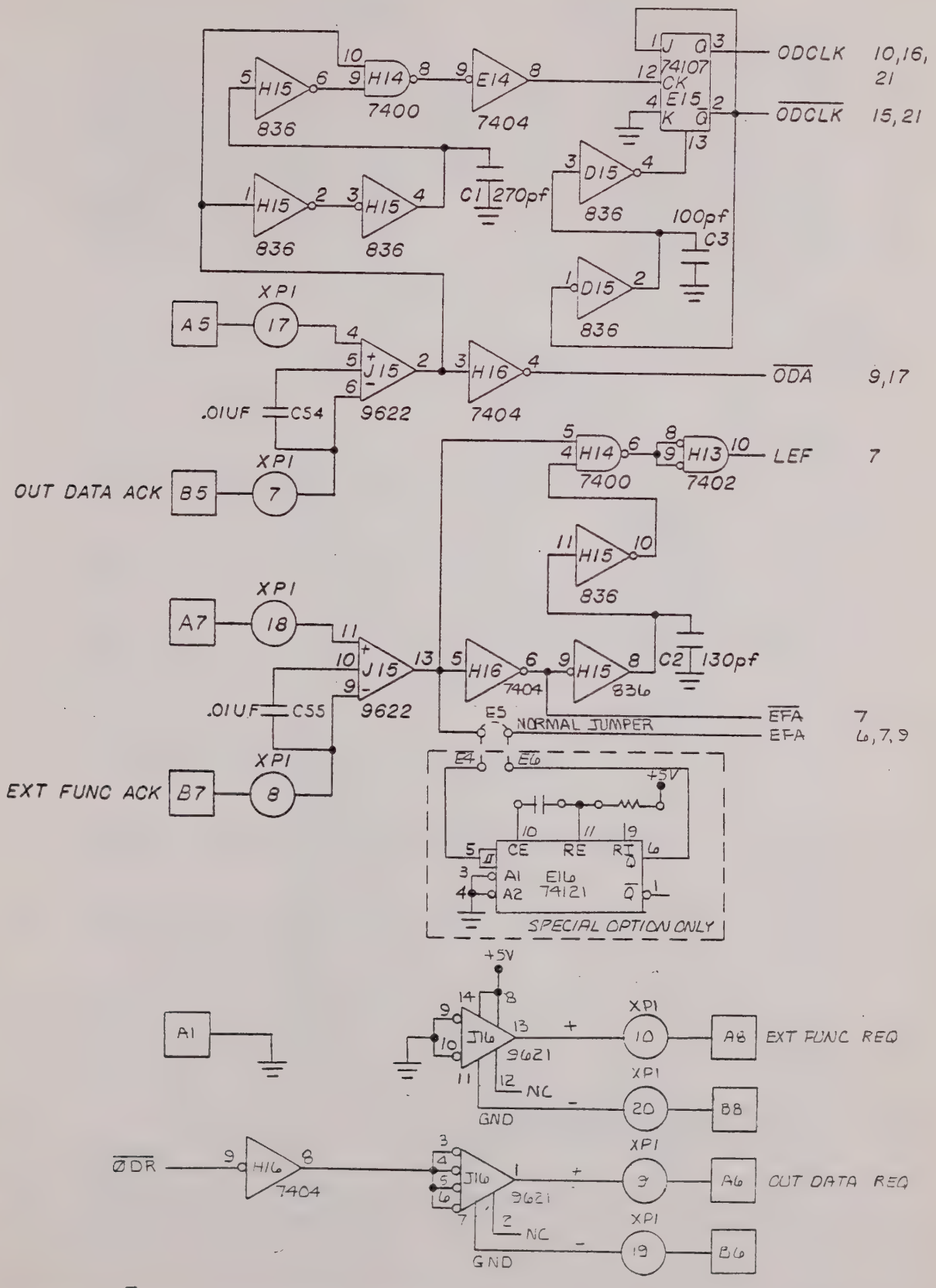
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H16
J15
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7402
9622
9621
C1 270pf
C2 130pf
C3 100pf
.01UF C54
.01UF C55
XP1
A5
17
A7
18
OUT DATA ACK B5
7
EXT FUNC ACK B7
8
ODA 9,17
LEF 7
EFA 7
EFA 6,7,9
E5 NORMAL JUMPER
E4
E6
+5V
CE
RE
RI
A1
A2
E16
74121
SPECIAL OPTION ONLY
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NC
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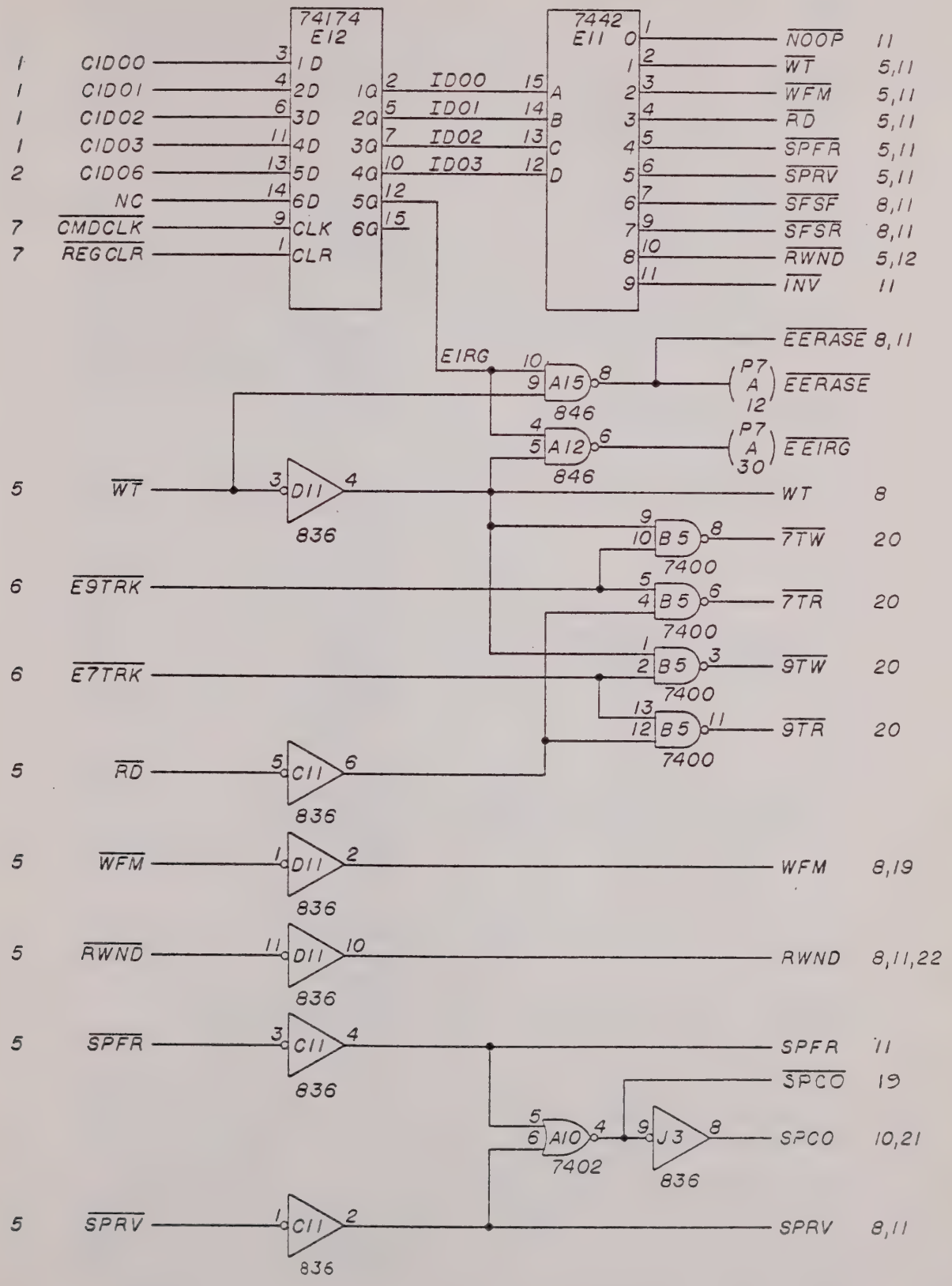
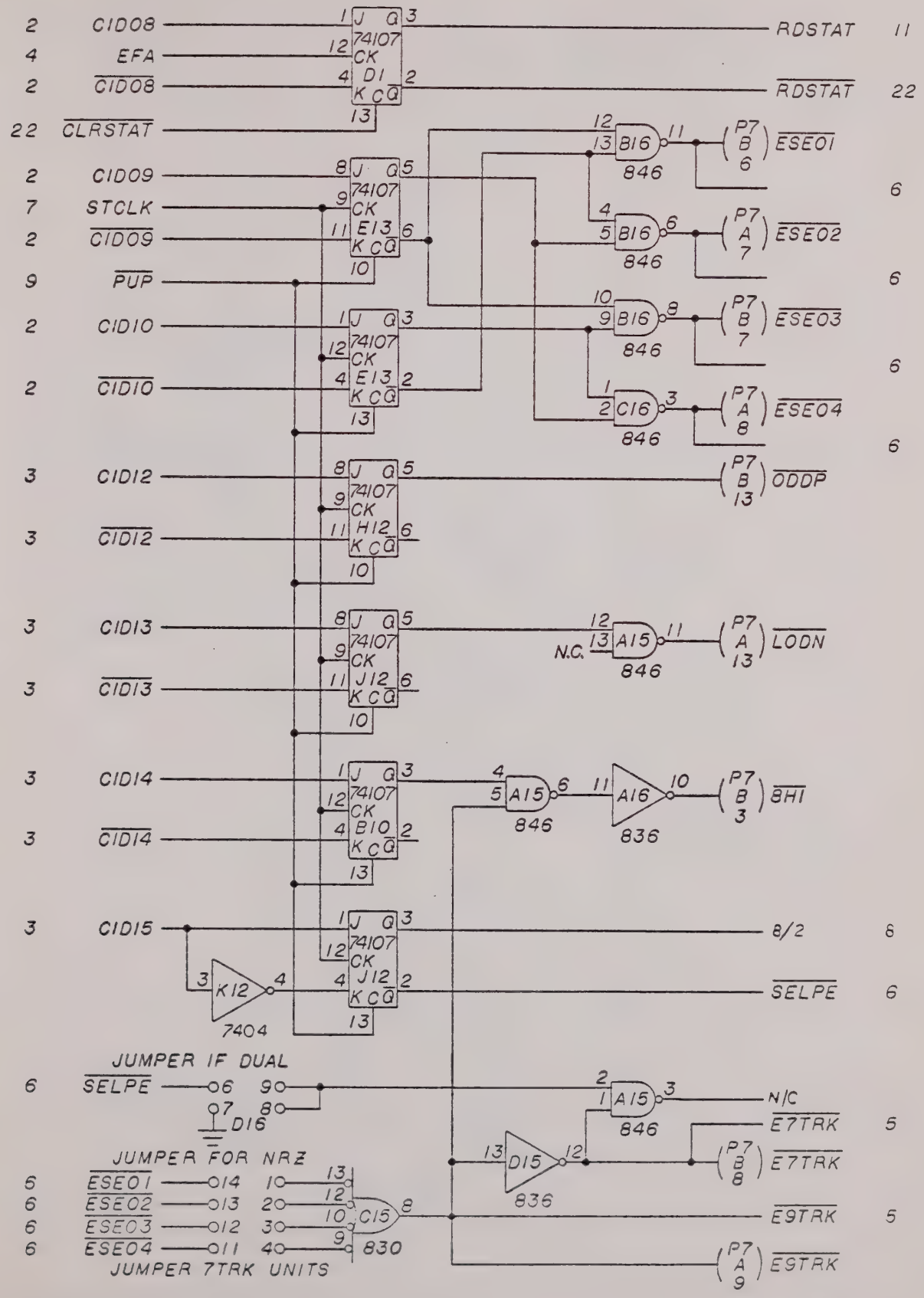
B8
ØDR
3
A6 OUT DATA REQ
B6
19



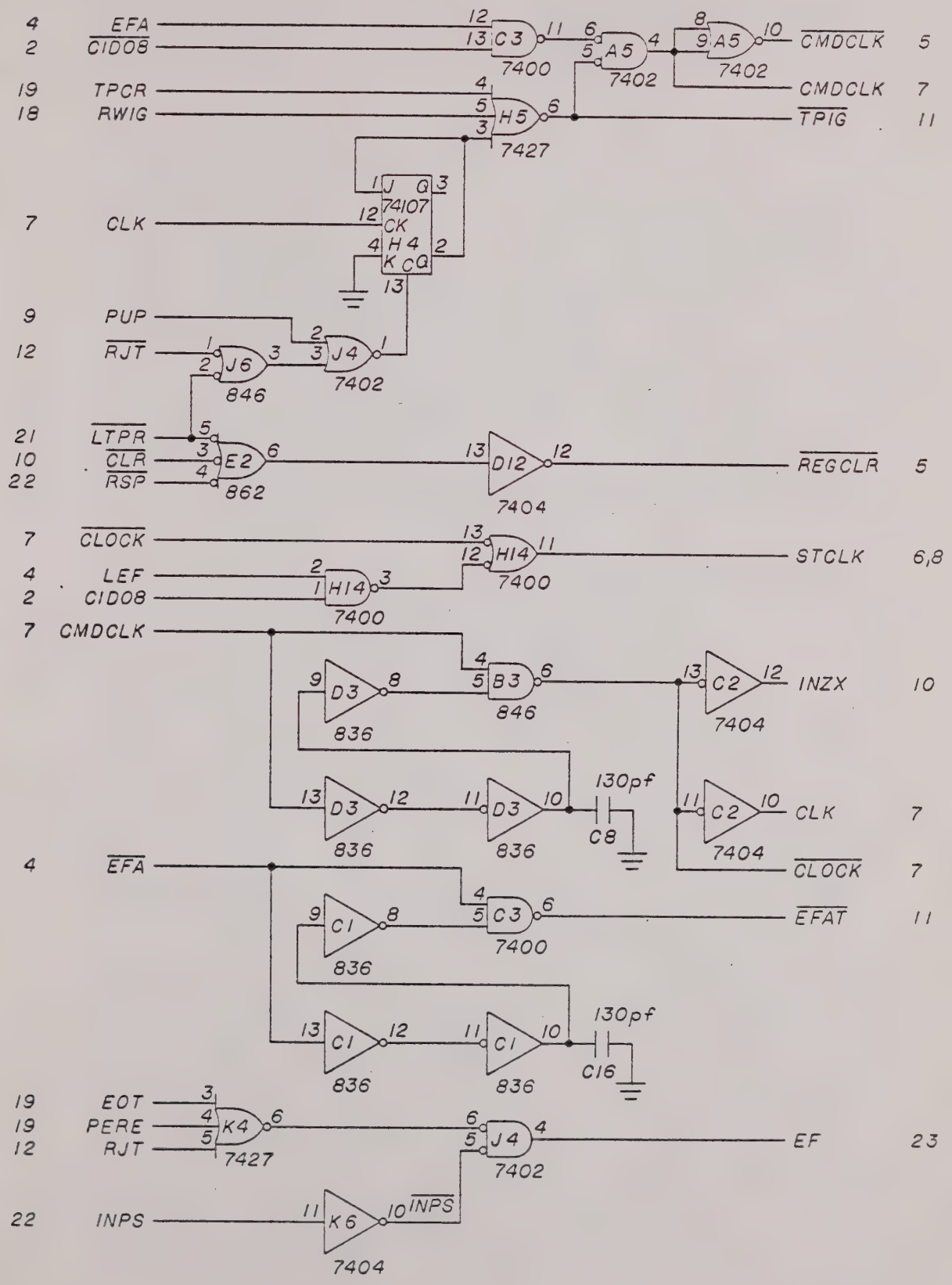
REV J

COMMAND AND SELECT REG 88003 SHEET 5



REV J

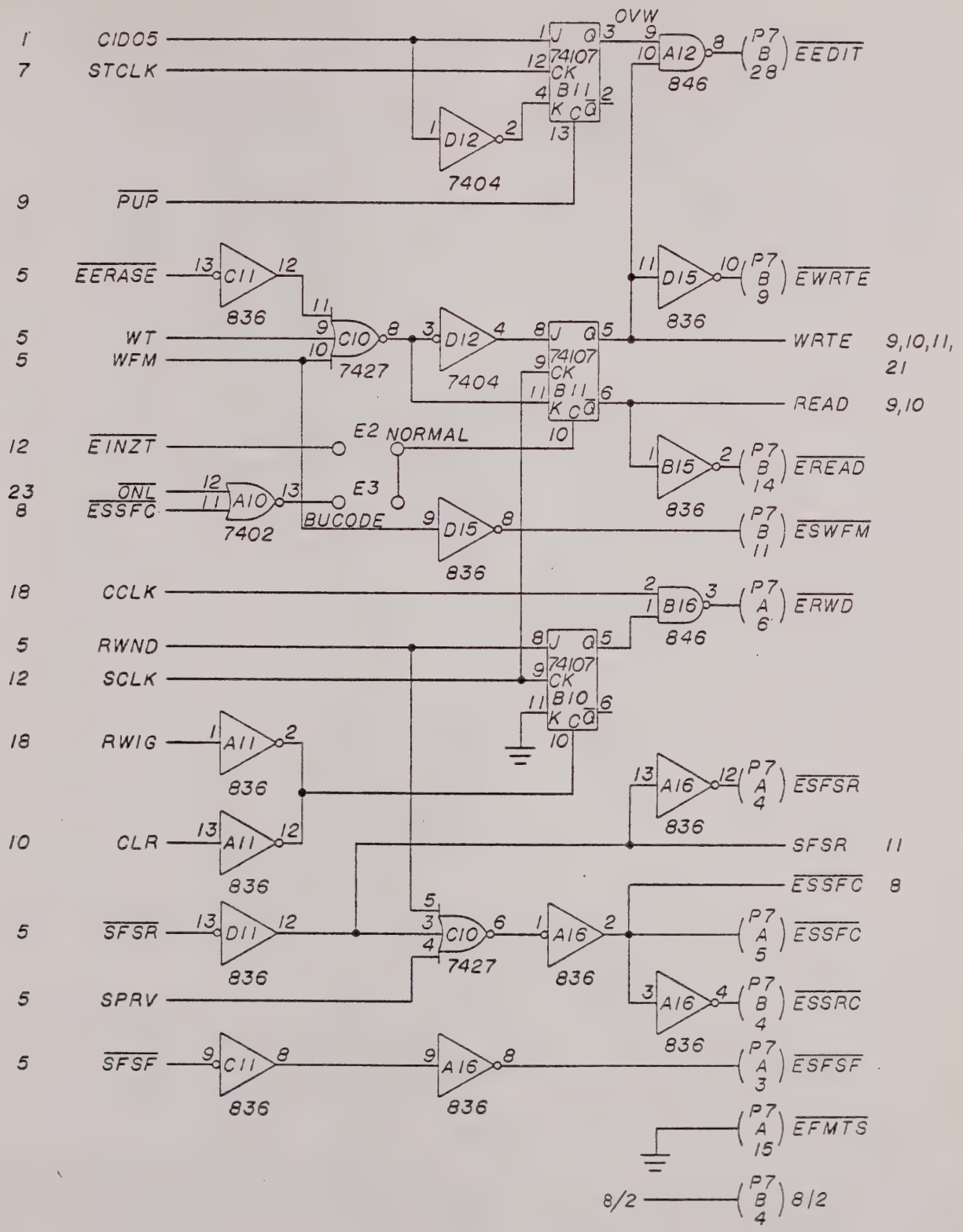
COMMAND AND SELECT REG 88003 SHEET 6



COMMAND TIMING

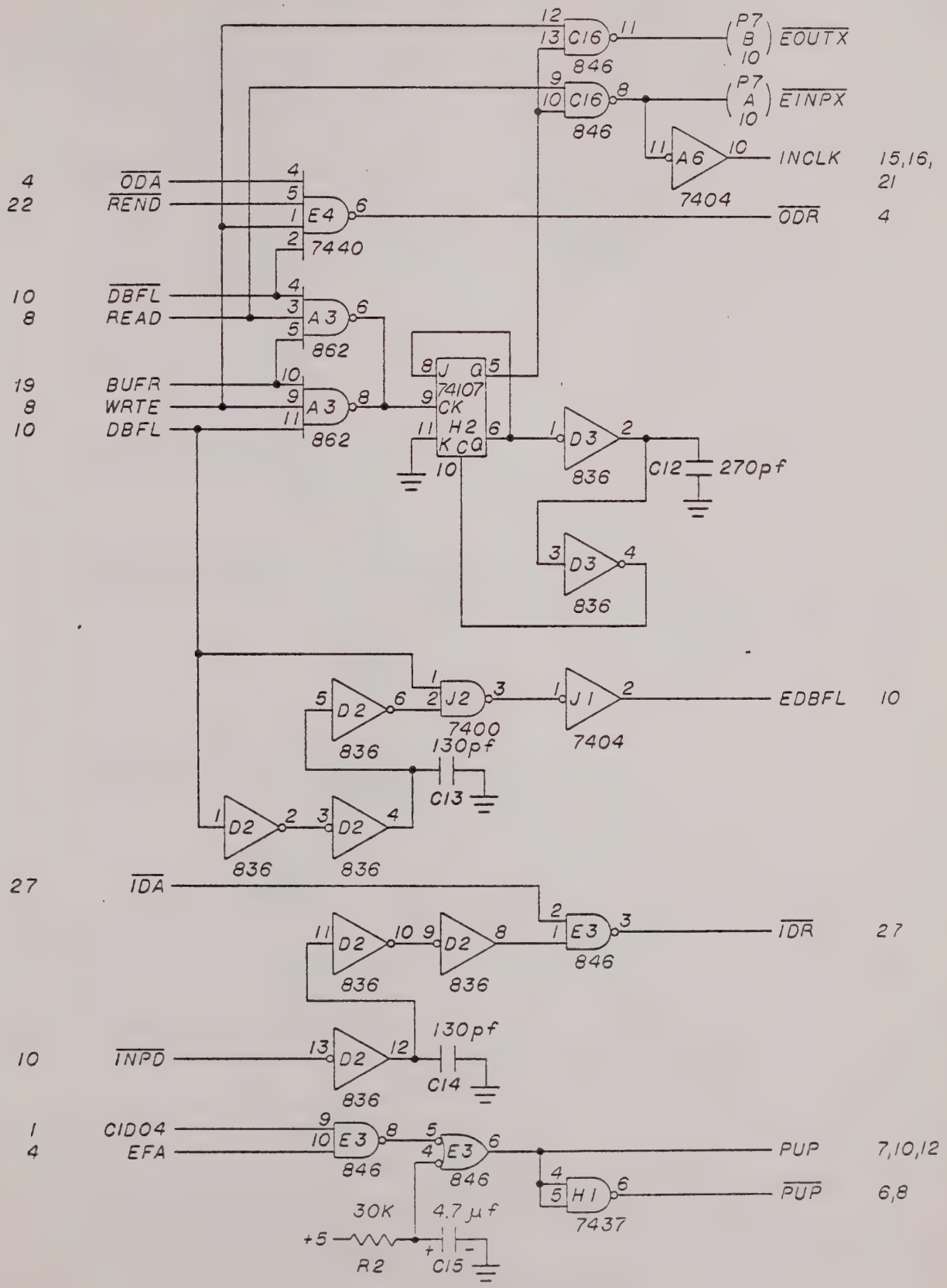
REV J

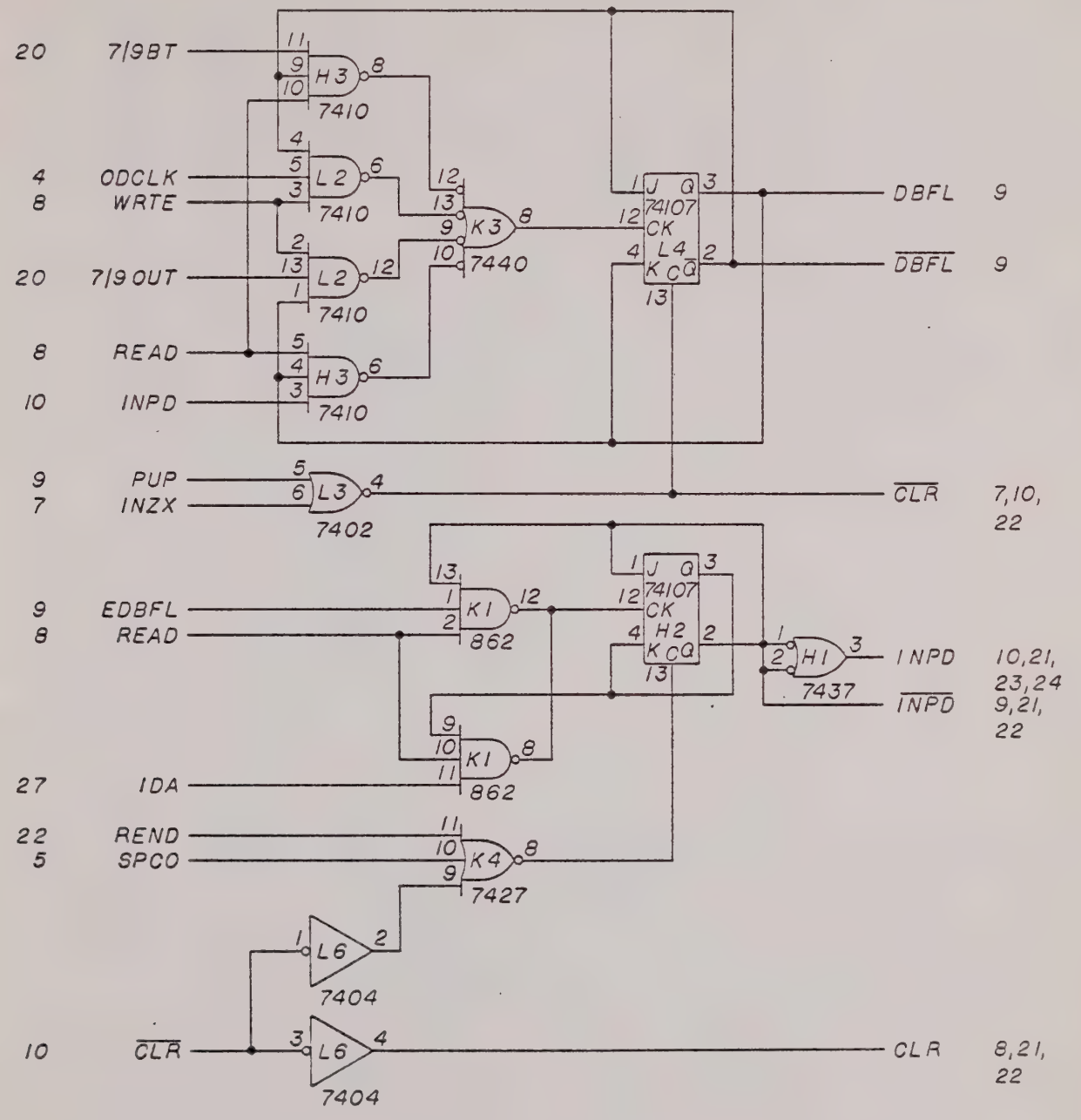
88003 SHEET 7

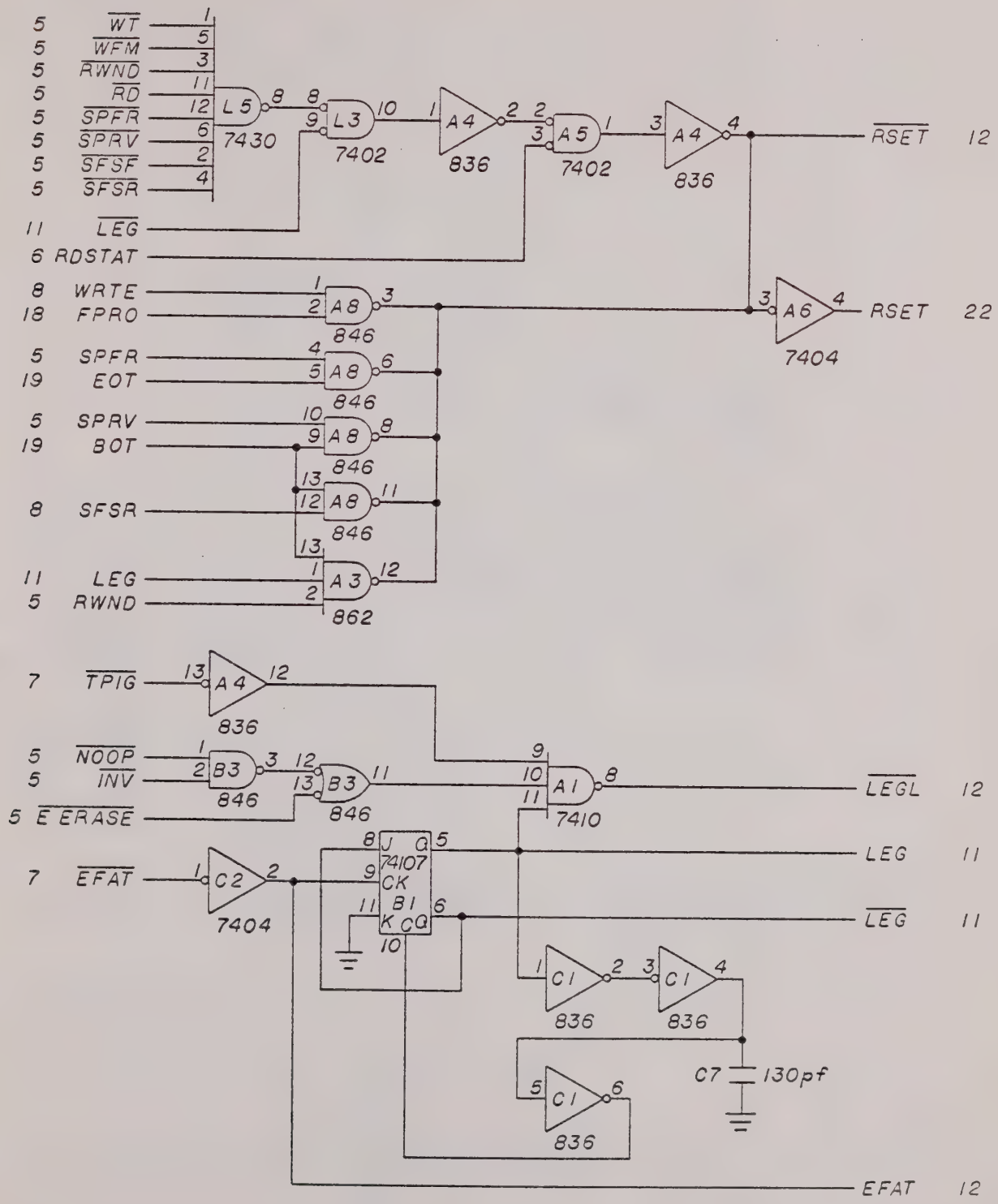


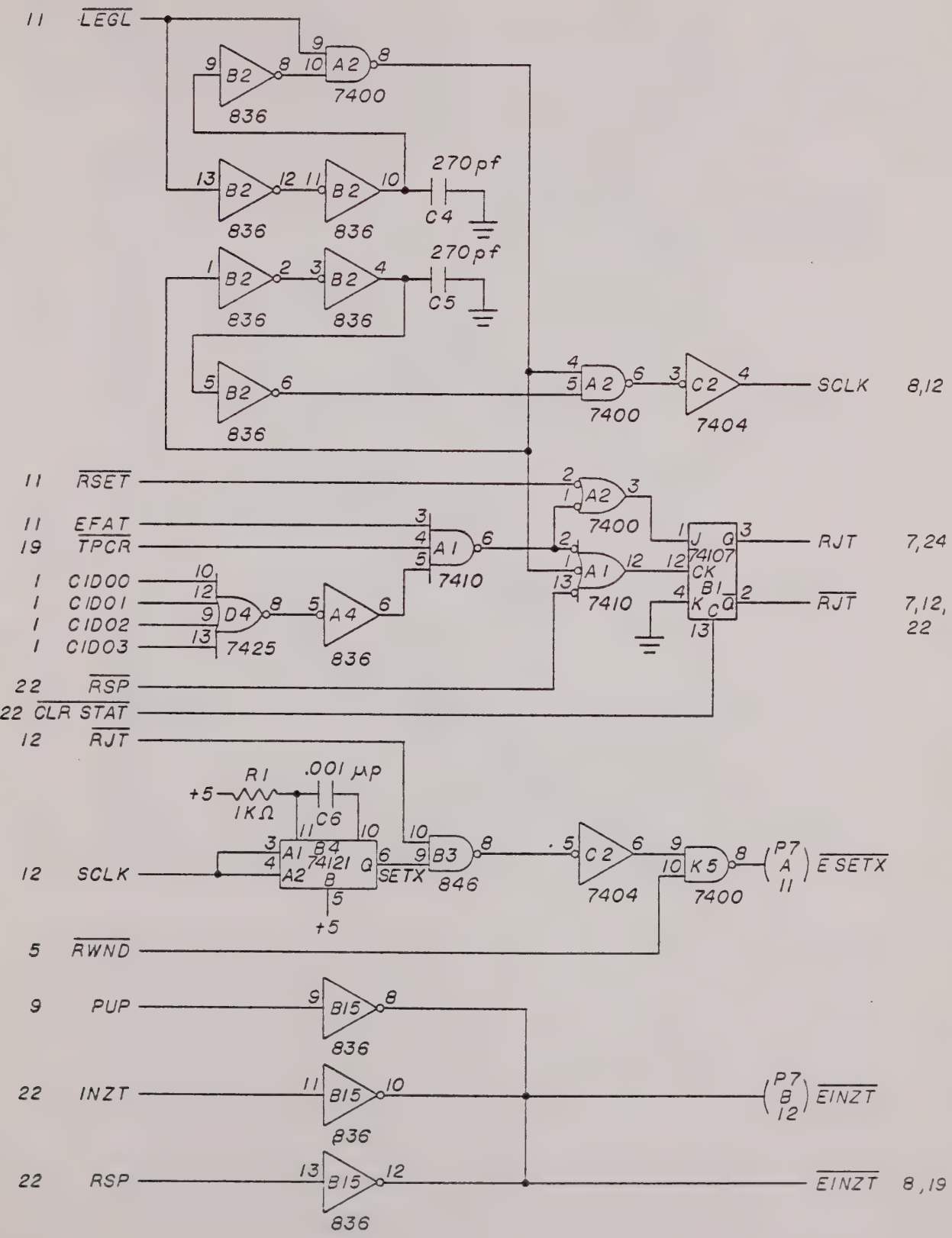
REV J

CONTROLS TO FORMATTER 88003 SHEET 8


C16
846
P7 B 10
EOUTX
P7 A 10
EINPX
A6
7404
INCLK
15,16, 21
4 ODA
22 REND
E4
7440
ODR
4
10 DBFL
8 READ
A3
862
19 BUFR
8 WRTE
10 DBFL
A3
862
74107
CK
H2
KCQ
D3
836
C12
270pf
D3
836
D2
836
J2
7400
J1
7404
EDBFL
10
130pf
C13
D2
836
D2
836
27 IDA
E3
846
IDR
27
D2
836
D2
836
130pf
10 INPD
D2
836
C14
1 CID04
4 EFA
E3
846
E3
846
PUP
7,10,12
H1
7437
PUP
6,8
30K
R2
4.7 μf
C15
+5


20 7/9BT
H3
7410
4 ODCLK
8 WRTE
L2
7410
20 7/9 OUT
L2
7410
8 READ
10 INPD
H3
7410
K3
7440
74107
CK
L4
DBFL 9
DBFL 9
9 PUP
7 INZX
L3
7402
CLR 7,10, 22
9 EDBFL
8 READ
K1
862
H2
H1
7437
INPD 10,21, 23,24
INPD 9,21, 22
27 IDA
K1
862
22 REND
5 SPCO
K4
7427
L6
7404
10 CLR
L6
7404
CLR 8,21, 22

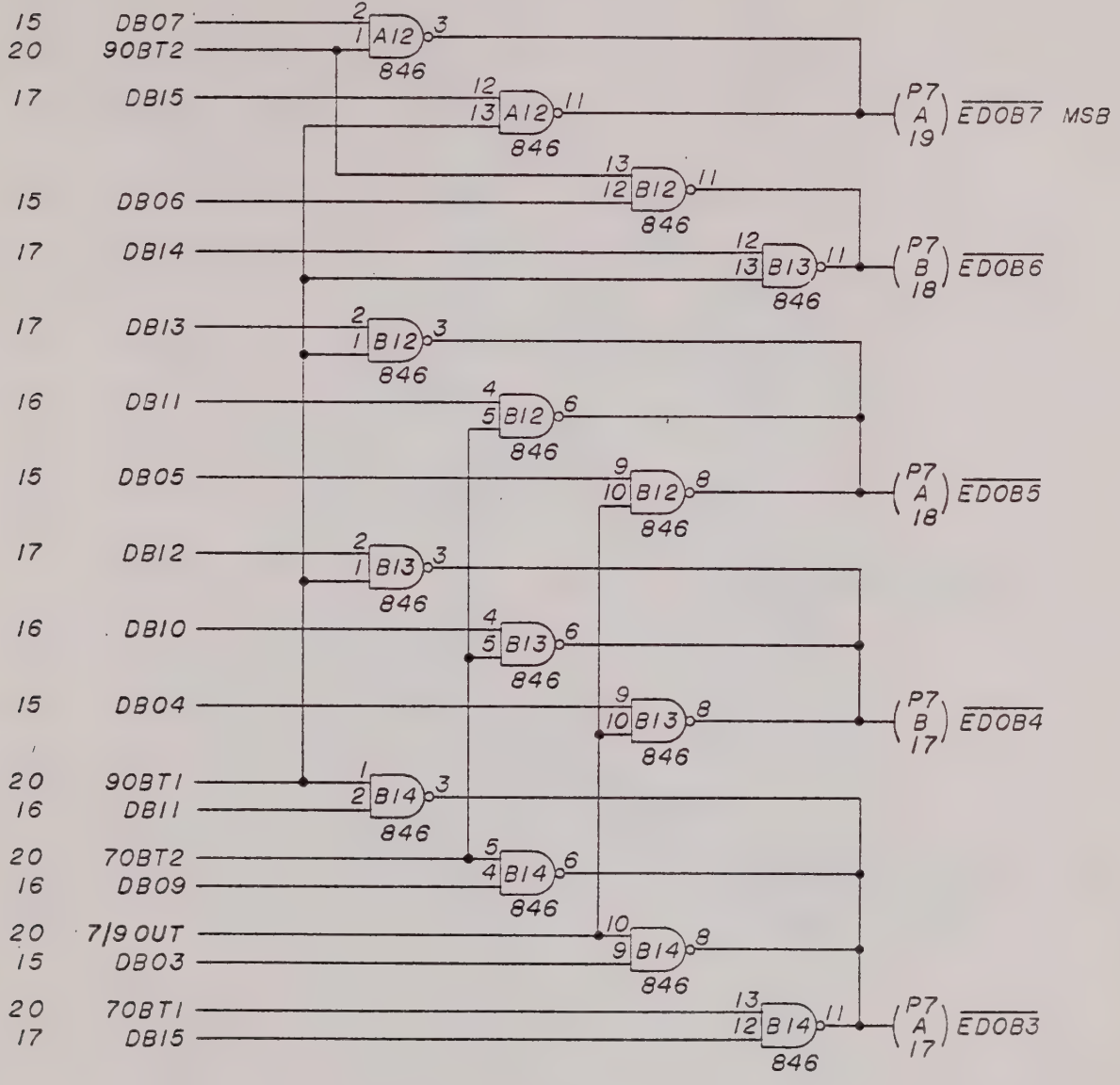

5 WT
5 WFM
5 RWND
5 RD
5 SPFR
5 SPRV
5 SFSF
5 SFSR
L 5
7430
L 3
7402
A 4
836
A 5
7402
A 4
836
RSET 12
11 LEG
6 RDSTAT
8 WRTE
18 FPRO
A 8
846
A 6
7404
RSET 22
5 SPFR
19 EOT
5 SPRV
19 BOT
8 SFSR
11 LEG
5 RWND
A 3
862
7 TPIG
A 4
836
5 NOOP
5 INV
5 E ERASE
B 3
846
A 1
7410
LEGL 12
7 EFAT
C 2
7404
74107
CK
B 1
K
LEG 11
LEG 11
C 1
836
C 1
836
C7 130pf
C 1
836
EFAT 12



COMMAND CLOCK AND REJECT

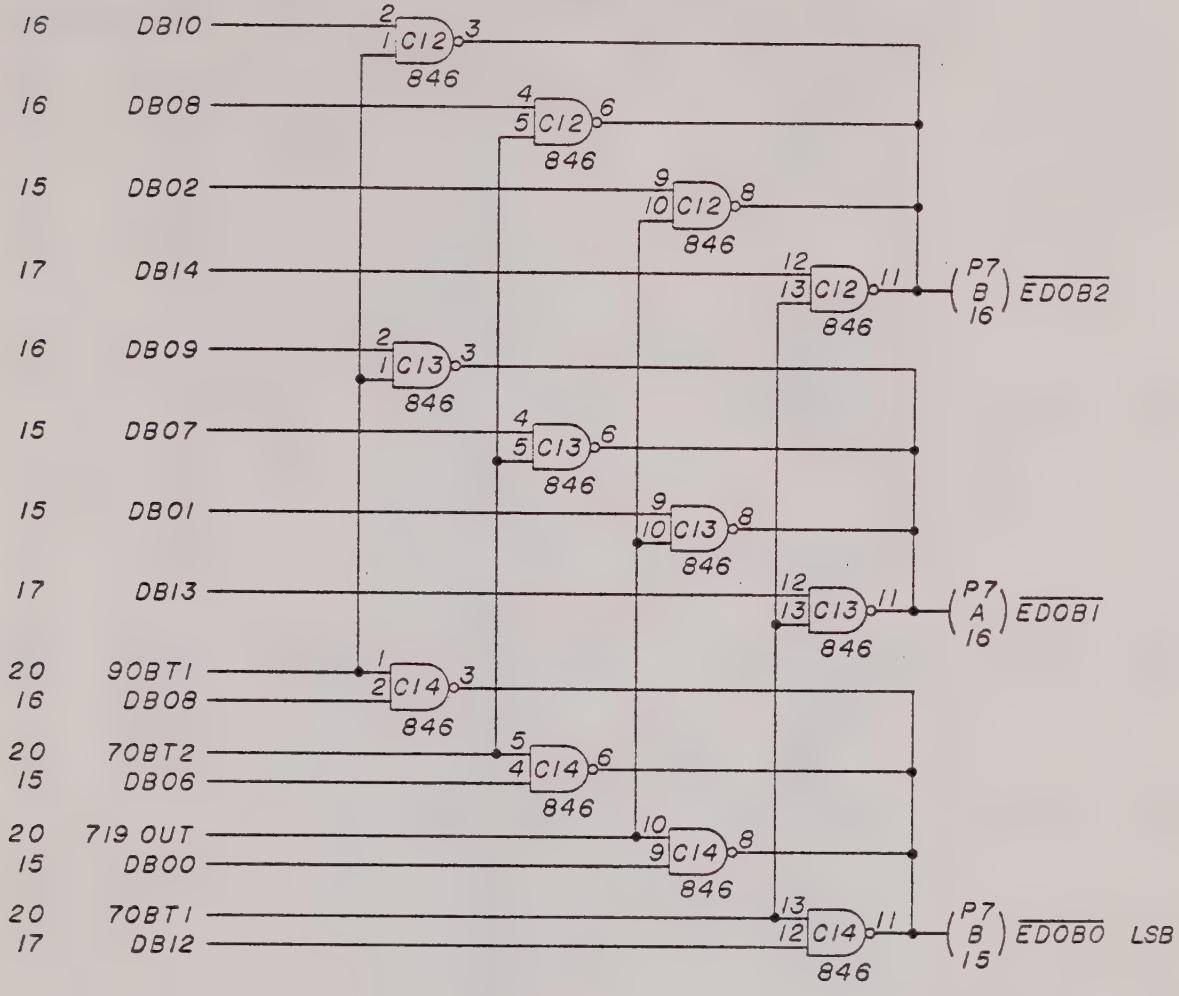
REV J

88003 SHEET 12

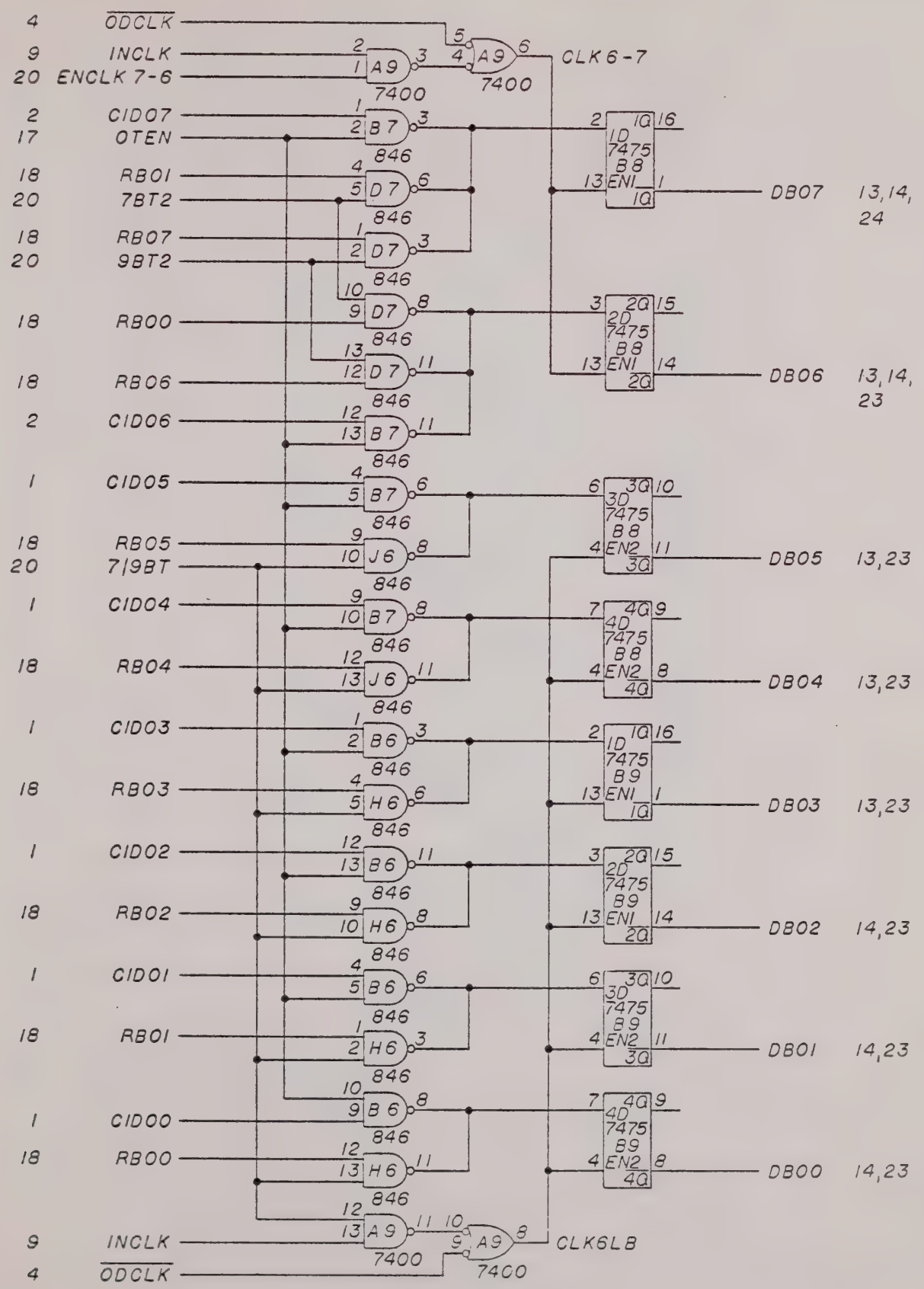


DATA OUTPUT GATING

REV J
88003 SHEET 13



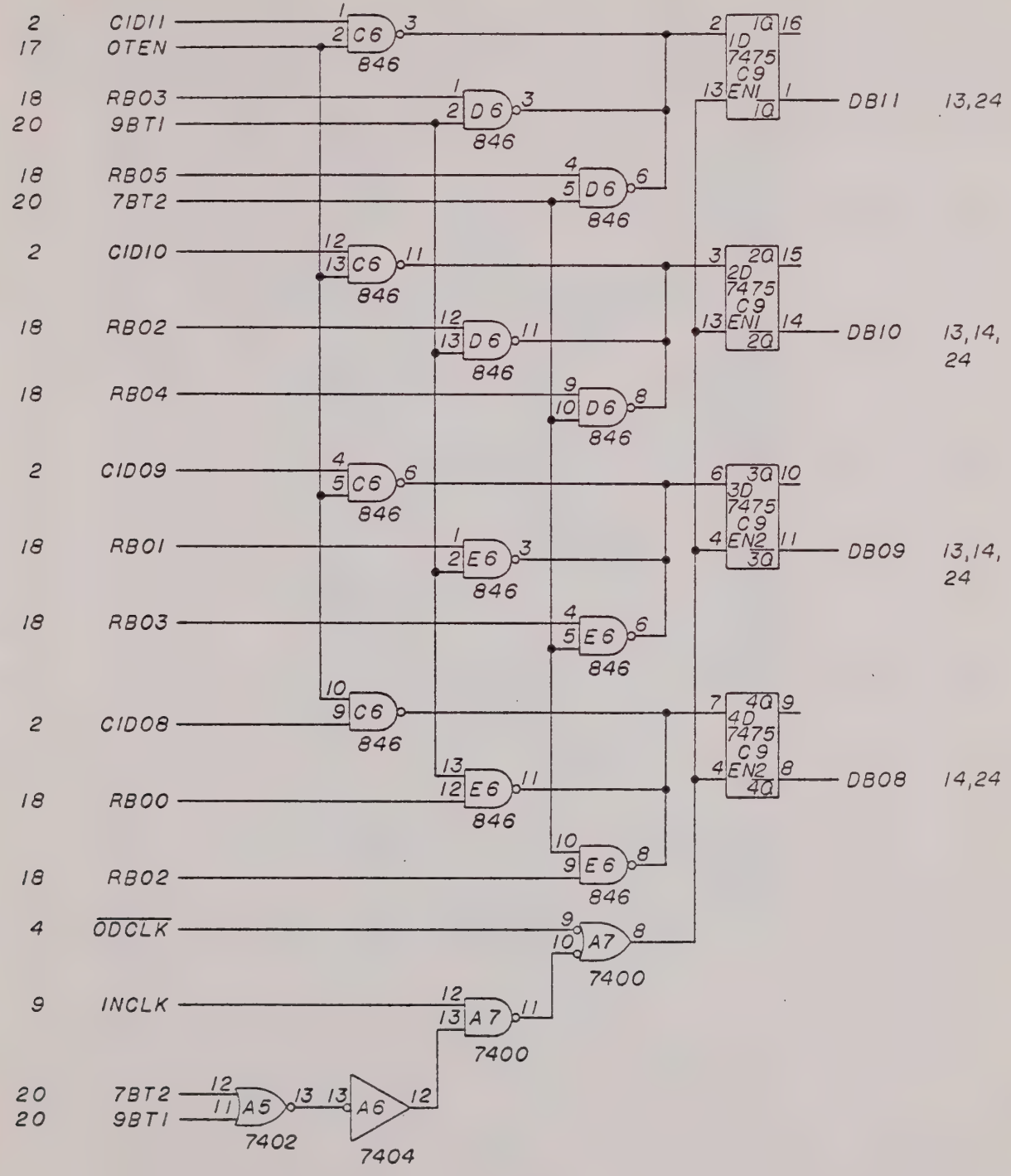
DATA OUTPUT GATING



REV J

DATA REGISTER

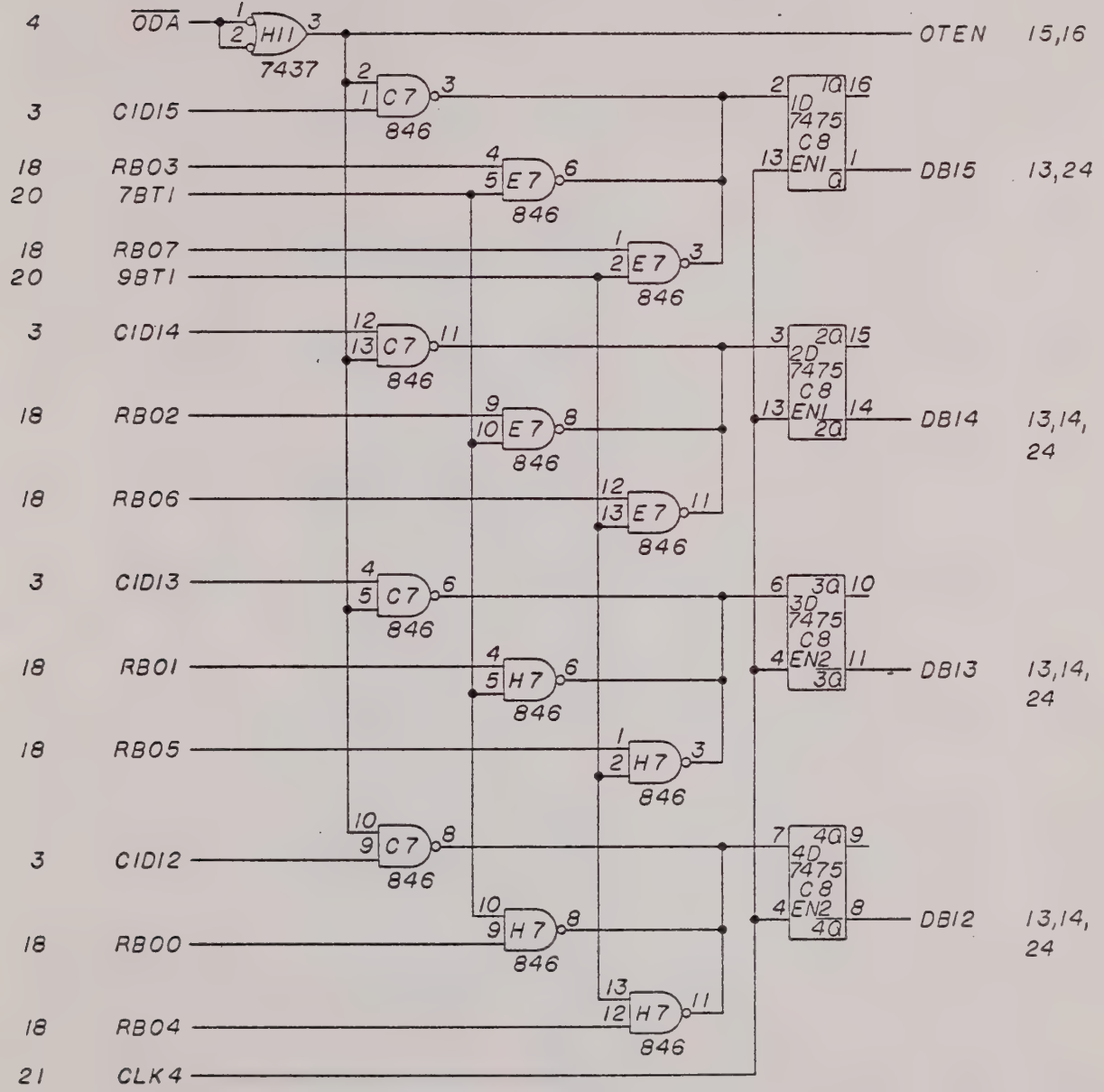
88003 SHEET 15

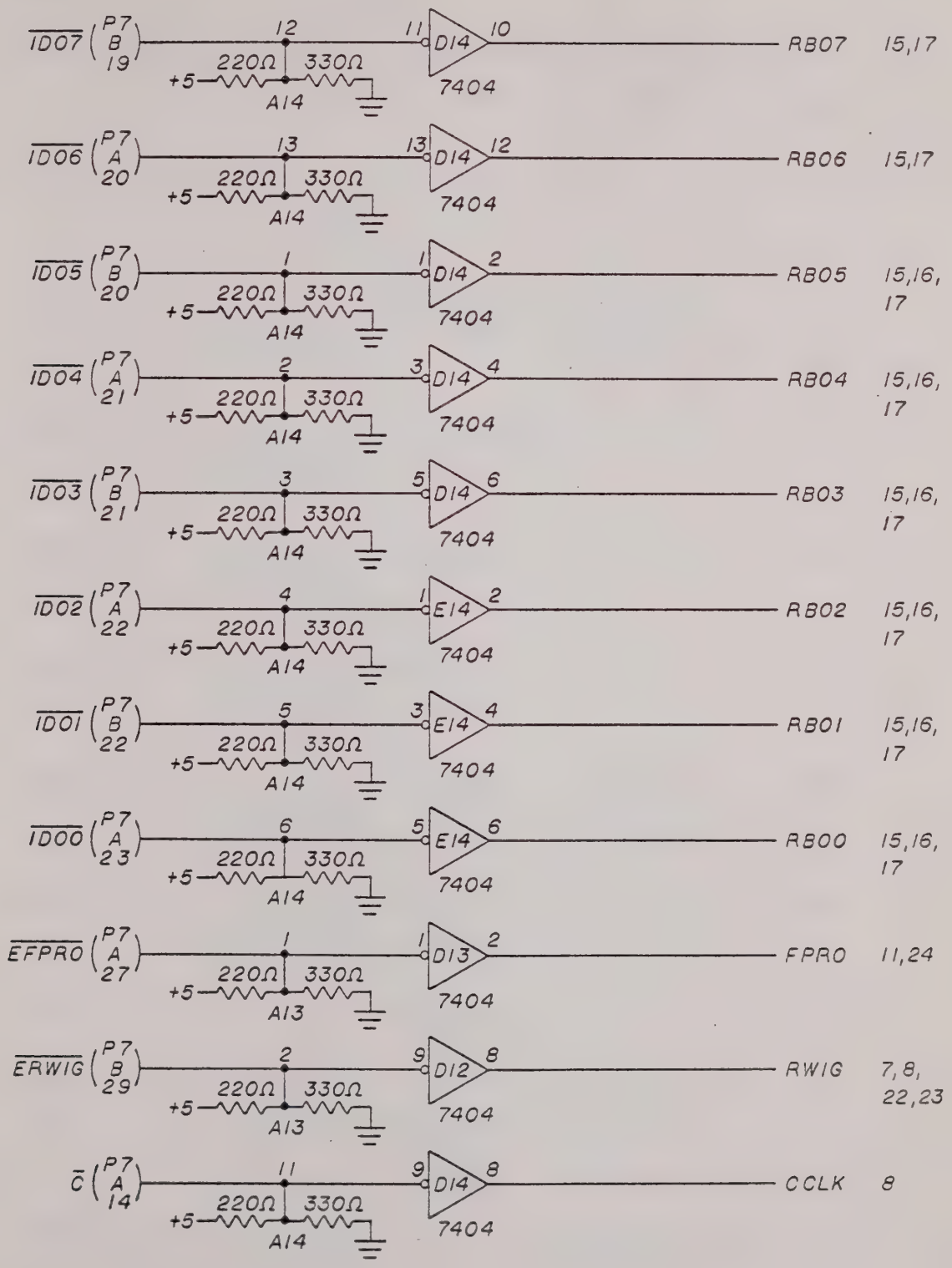


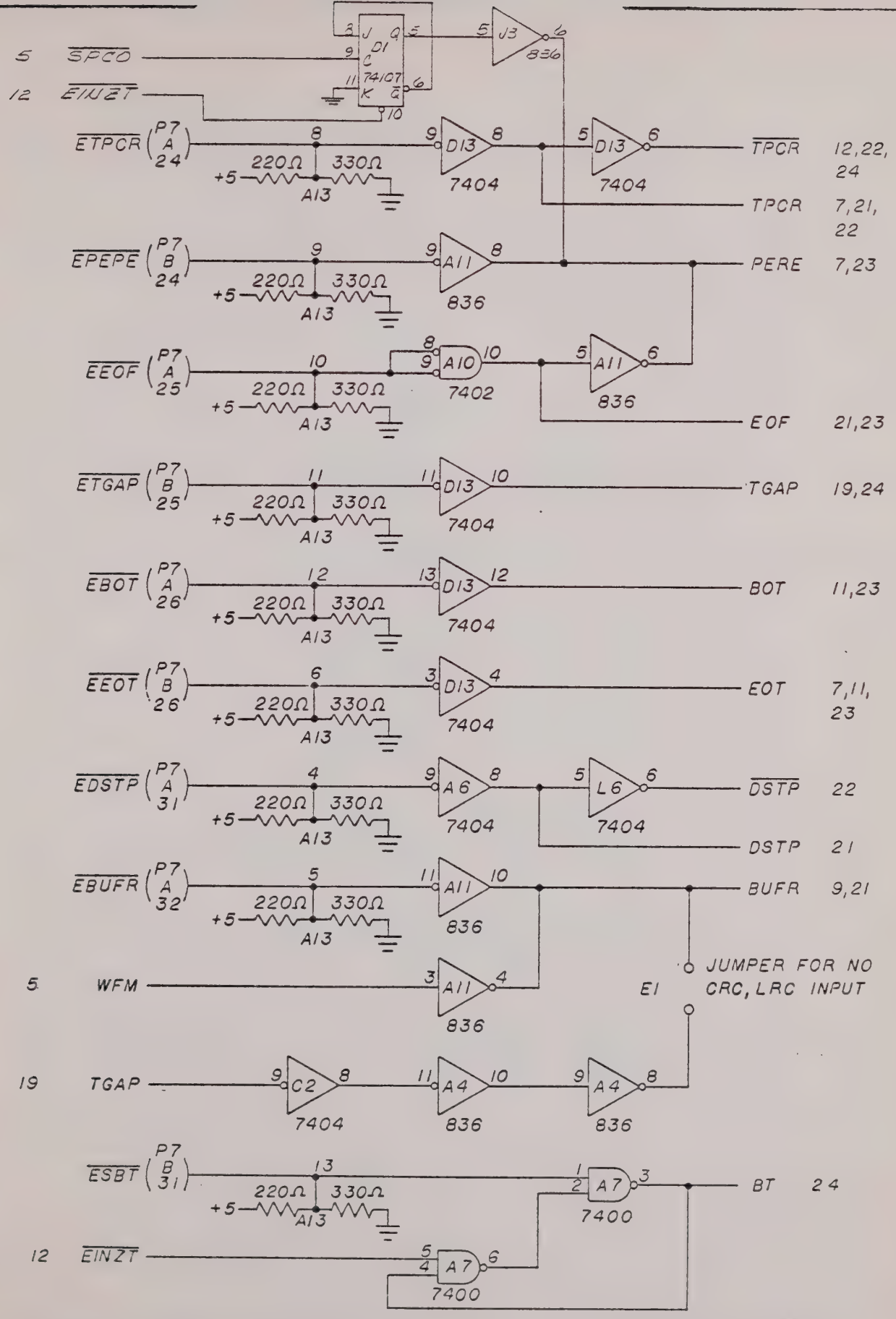
DATA REGISTER

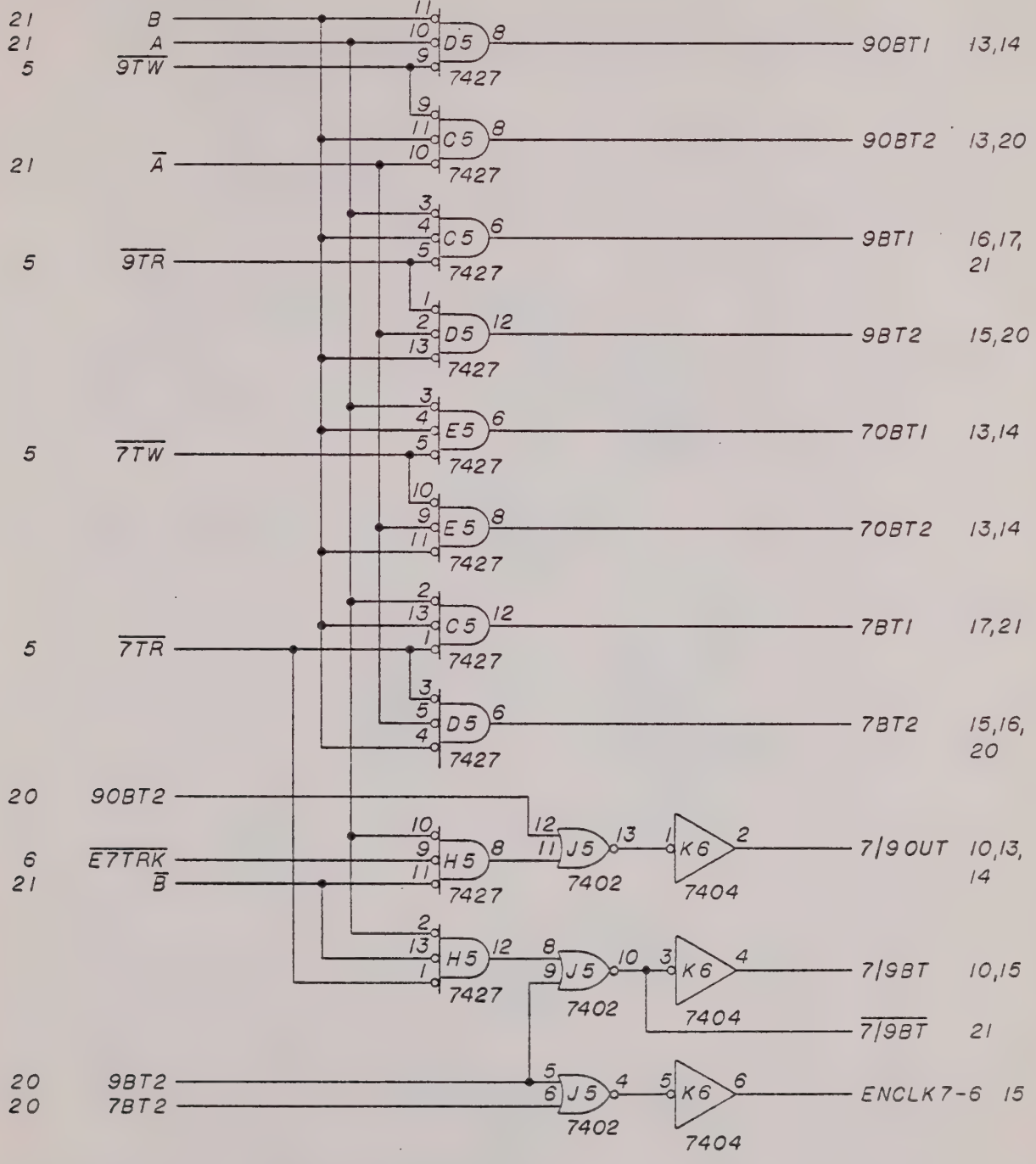
REV J

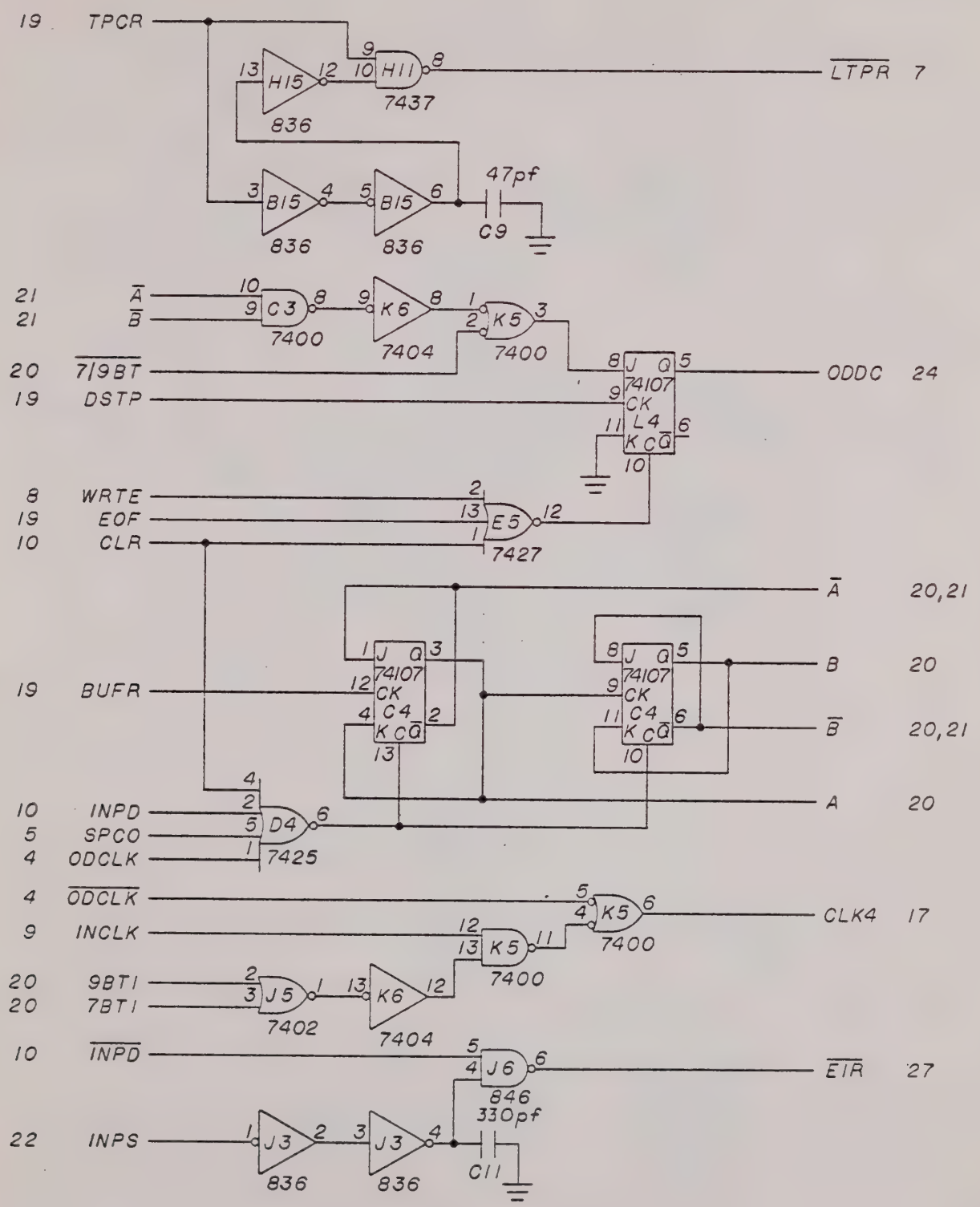
88003 SHEET 16

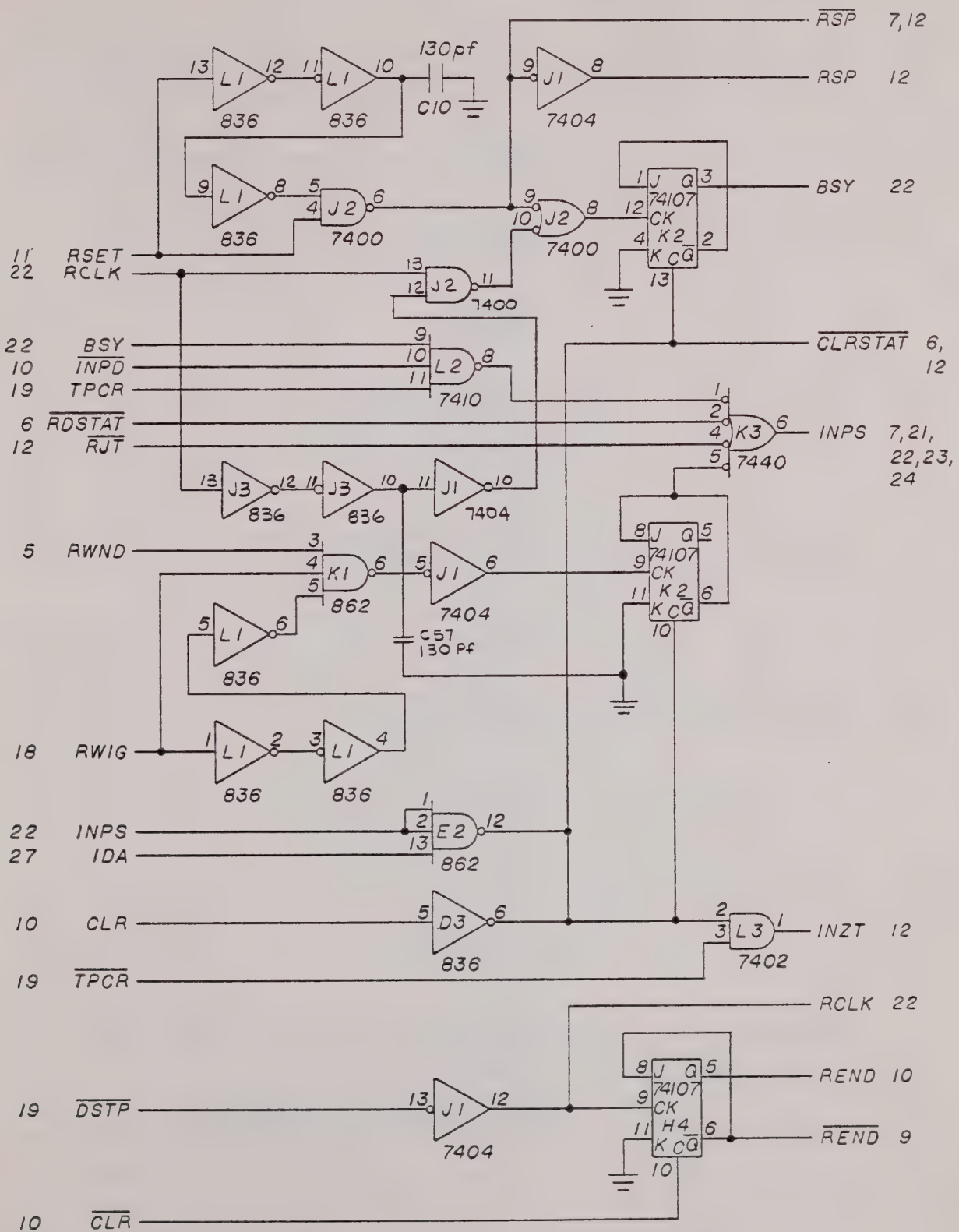

4 ODA
H11
7437
OTEN 15,16
3 CIDI5
C7
846
18 RB03
20 7BTI
E7
846
18 RB07
20 9BTI
E7
846
3 CIDI4
C7
846
18 RB02
E7
846
18 RB06
E7
846
3 CIDI3
C7
846
18 RB01
H7
846
18 RB05
H7
846
3 CIDI2
C7
846
18 RB00
H7
846
18 RB04
H7
846
21 CLK4
1D 7475 C8
ENI
DB15 13,24
2D 7475 C8
EN1
DB14 13,14, 24
3D 7475 C8
EN2
DB13 13,14, 24
4D 7475 C8
EN2
DB12 13,14, 24

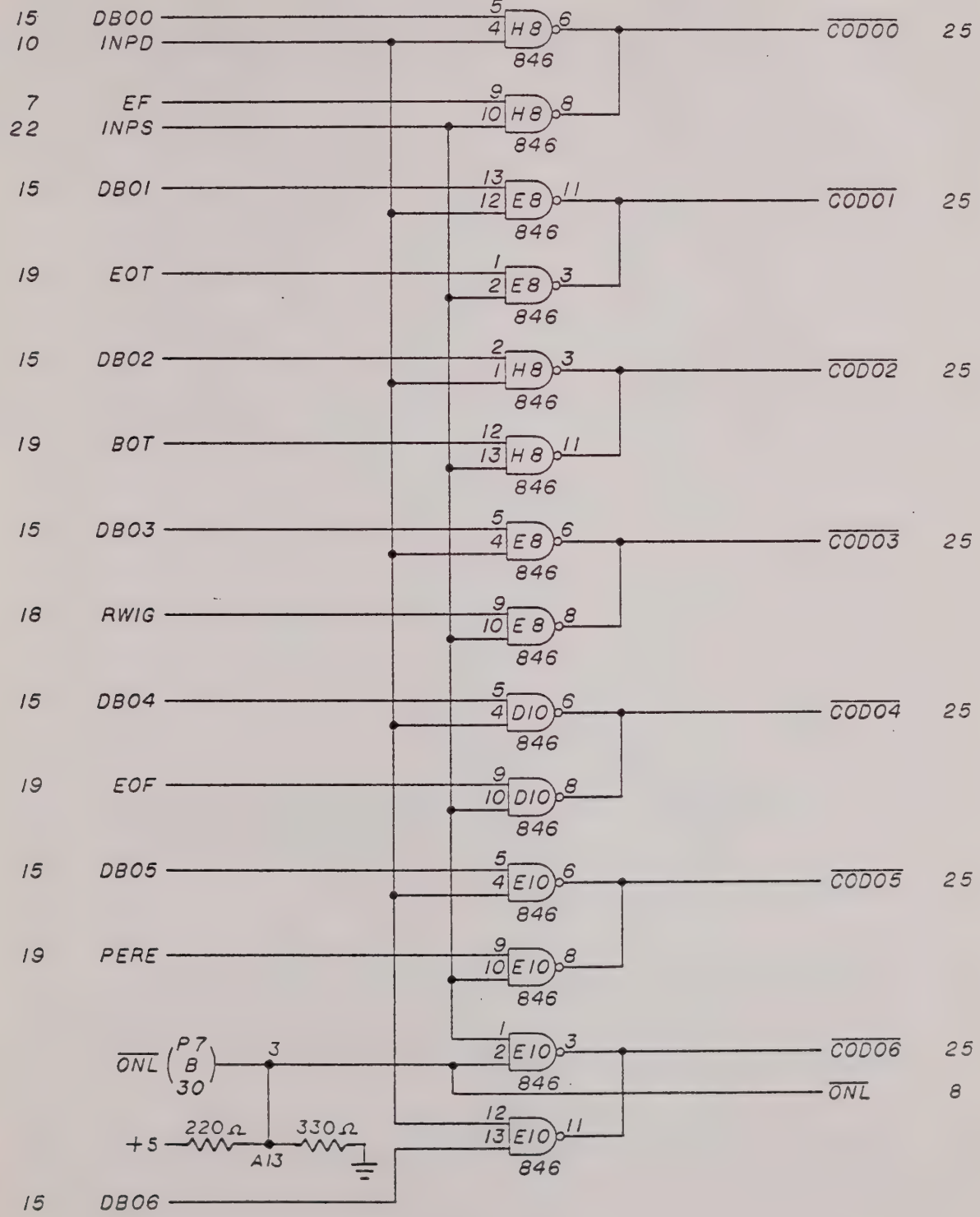

IDO7 (P7 B 19) 12 11 D14 10 RB07 15,17
IDO6 (P7 A 20) 13 13 D14 12 RB06 15,17
IDO5 (P7 B 20) 1 1 D14 2 RB05 15,16, 17
IDO4 (P7 A 21) 2 3 D14 4 RB04 15,16, 17
IDO3 (P7 B 21) 3 5 D14 6 RB03 15,16, 17
IDO2 (P7 A 22) 4 1 E14 2 RB02 15,16, 17
IDO1 (P7 B 22) 5 3 E14 4 RB01 15,16, 17
IDO0 (P7 A 23) 6 5 E14 6 RB00 15,16, 17
EFPRO (P7 A 27) 1 1 D13 2 FPRO 11,24
ERWIG (P7 B 29) 2 9 D12 8 RWIG 7,8, 22,23
C (P7 A 14) 11 9 D14 8 CCLK 8
220Ω 330Ω +5 A14
A13
7404

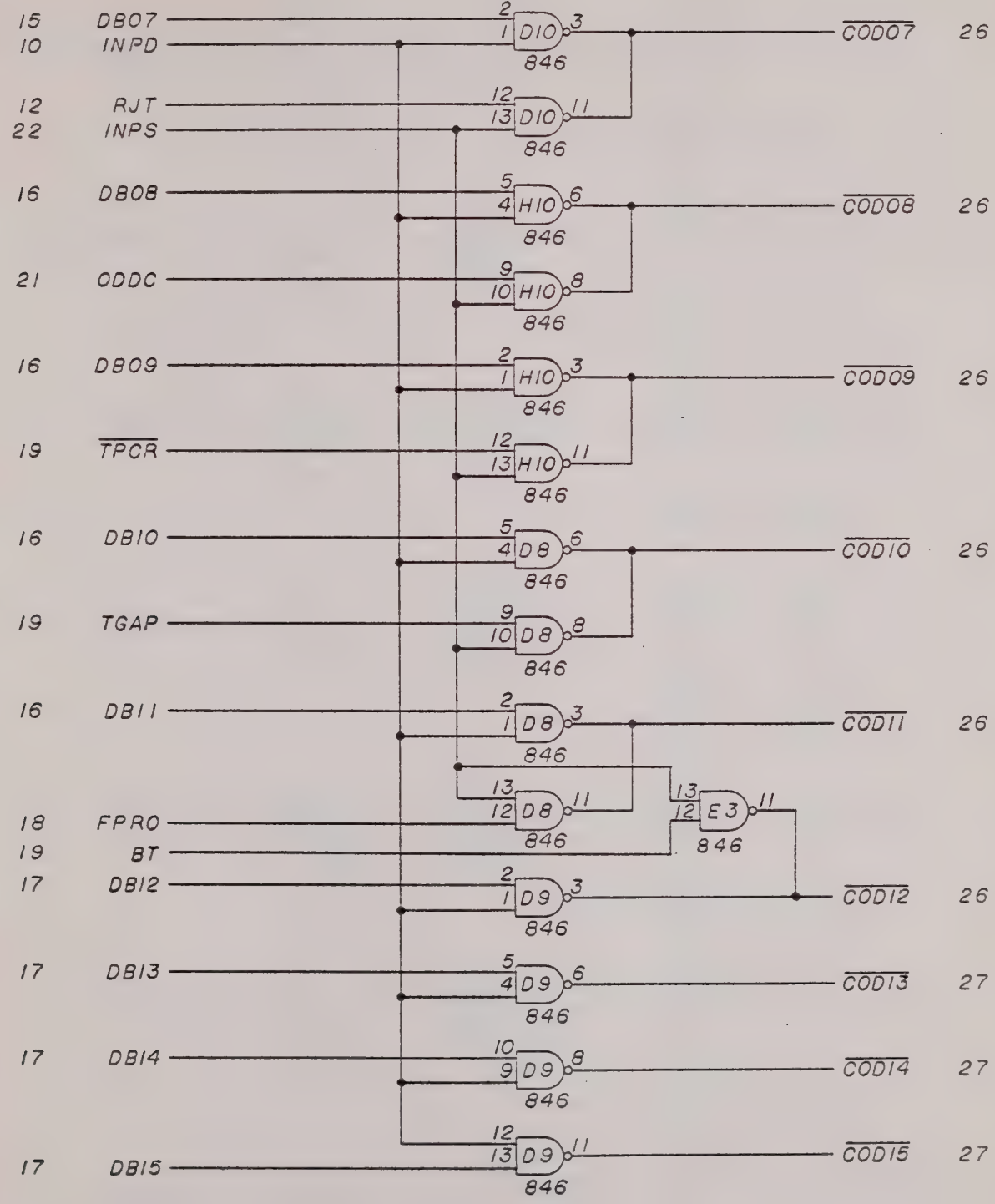

5 SPCO
12 EINZT
74107
J1 836
ETPCR (P7 A 24)
EPEPE (P7 B 24)
EEOF (P7 A 25)
ETGAP (P7 B 25)
EBOT (P7 A 26)
EEOT (P7 B 26)
EDSTP (P7 A 31)
EBUFR (P7 A 32)
220Ω 330Ω +5 A13
D13 7404
A11 836
A10 7402
A6 7404
L6 7404
5 WFM
19 TGAP
C2 7404
A4 836
ESBT (P7 B 31)
A7 7400
TPCR 12,22, 24
TPCR 7,21, 22
PERE 7,23
EOF 21,23
TGAP 19,24
BOT 11,23
EOT 7,11, 23
DSTP 22
DSTP 21
BUFR 9,21
E1 JUMPER FOR NO CRC, LRC INPUT
BT 24


21 B
21 A
5 9TW
D5
7427
90BT1 13,14
9 11 C5 10
21 Ā
7427
90BT2 13,20
3 4 C5 5
5 9TR
7427
9BT1 16,17, 21
1 2 D5 13
7427
9BT2 15,20
3 4 E5 5
5 7TW
7427
70BT1 13,14
10 9 E5 11
7427
70BT2 13,14
2 13 C5 1
5 7TR
7427
7BT1 17,21
3 5 D5 4
7427
7BT2 15,16, 20
20 90BT2
10 9 H5 11
6 E7TRK
21 B̄
7427
12 11 J5 13
7402
1 K6 2
7404
7/9 OUT 10,13, 14
2 13 H5 1
7427
12 8 9 J5 10
7402
3 K6 4
7404
7/9BT 10,15
7/9BT 21
20 9BT2
20 7BT2
5 6 J5 4
7402
5 K6 6
7404
ENCLK7-6 15


19 TPCR
H15
H11
7437
836
LTPR 7
B15
B15
836
836
47pf
C9
21 A
21 B
C3
7400
K6
7404
K5
7400
20 7/9BT
19 DSTP
74107
L4
ODDC 24
8 WRTE
19 EOF
10 CLR
E5
7427
A 20,21
B 20
B 20,21
A 20
19 BUFR
74107
C4
10 INPD
5 SPCO
4 ODCLK
D4
7425
4 ODCLK
9 INCLK
K5
7400
CLK4 17
20 9BTI
20 7BTI
J5
7402
K6
7404
10 INPD
J6
846
EIR 27
330pf
22 INPS
J3
836
C11

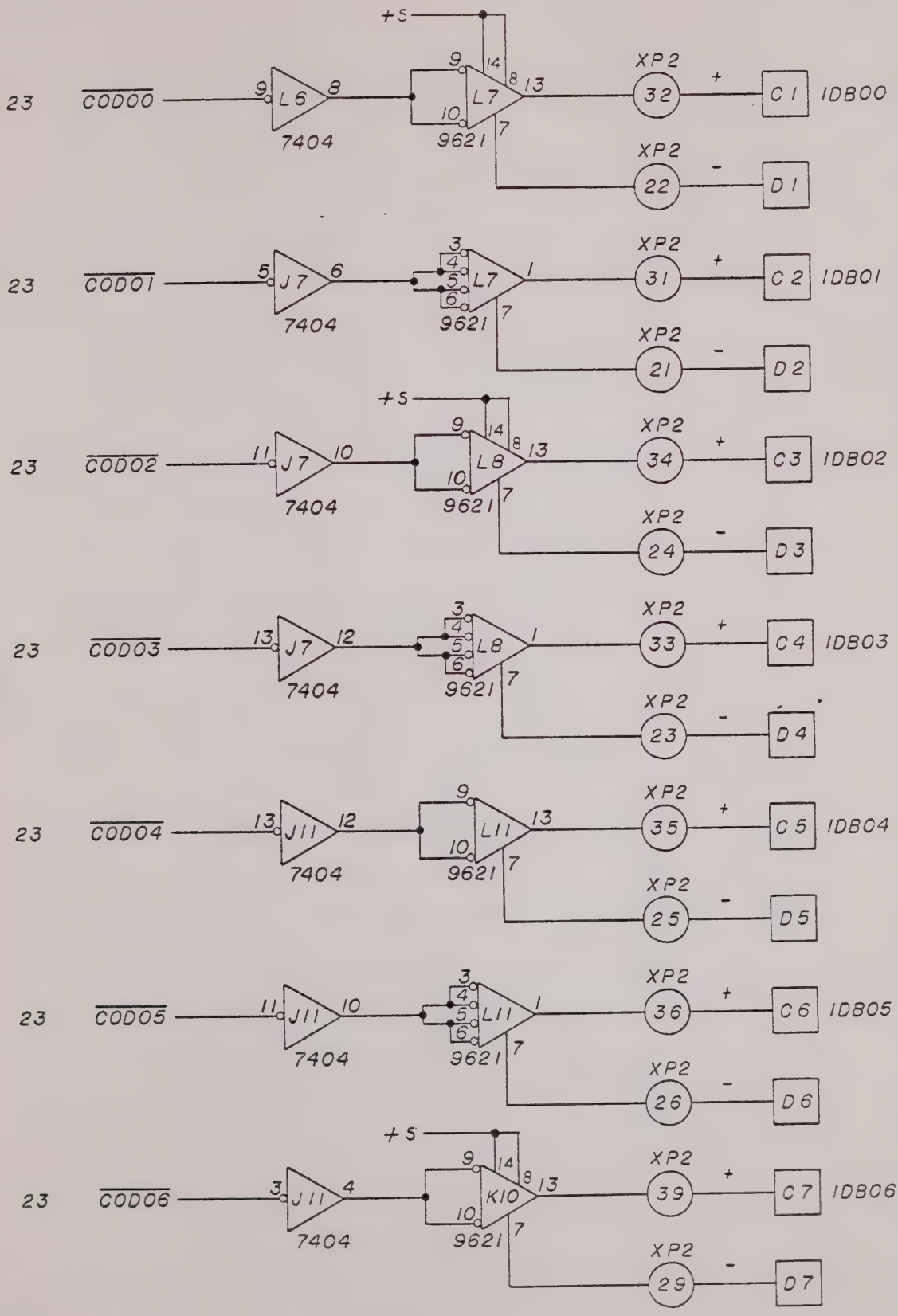

RSP 7,12
RSP 12
130pf
C10
L1
836
J1
7404
BSY 22
74107
CK
K2
J2
7400
11 RSET
22 RCLK
CLRSTAT 6, 12
22 BSY
10 INPD
19 TPCR
L2
7410
6 RDSTAT
12 RJT
K3
7440
INPS 7,21, 22,23, 24
J3
836
5 RWND
K1
862
C57
130 pf
18 RWIG
22 INPS
27 IDA
E2
862
10 CLR
D3
836
L3
7402
INZT 12
19 TPCR
RCLK 22
19 DSTP
H4
REND 10
REND 9
10 CLR

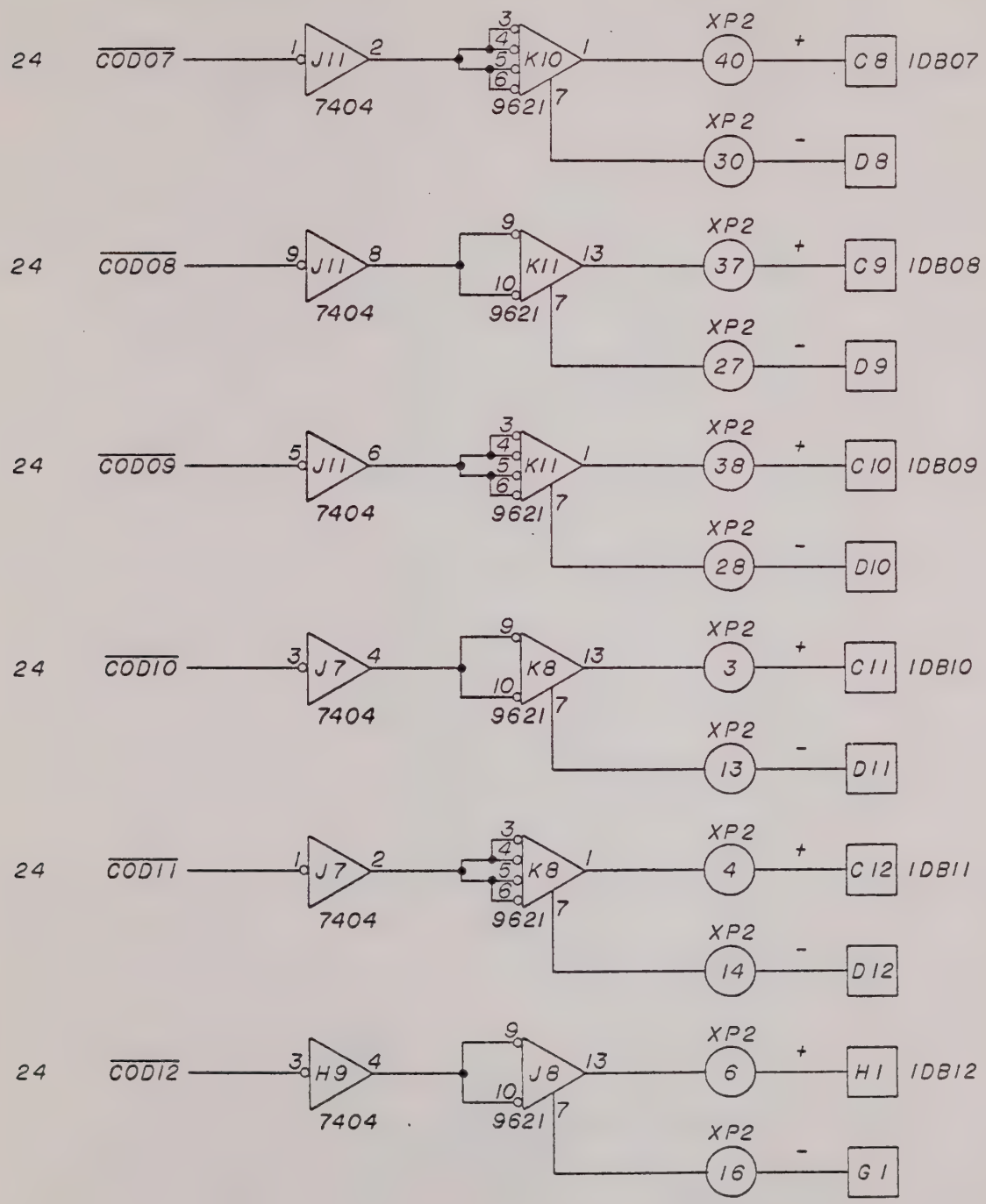

15 DB00
10 INPD
7 EF
22 INPS
15 DB01
19 EOT
15 DB02
19 BOT
15 DB03
18 RWIG
15 DB04
19 EOF
15 DB05
19 PERE
ONL (P7 B 30)
+5
220Ω
330Ω
A13
15 DB06
H8 846
E8 846
D10 846
E10 846
CODO0 25
CODO1 25
CODO2 25
CODO3 25
CODO4 25
CODO5 25
CODO6 25
ONL 8

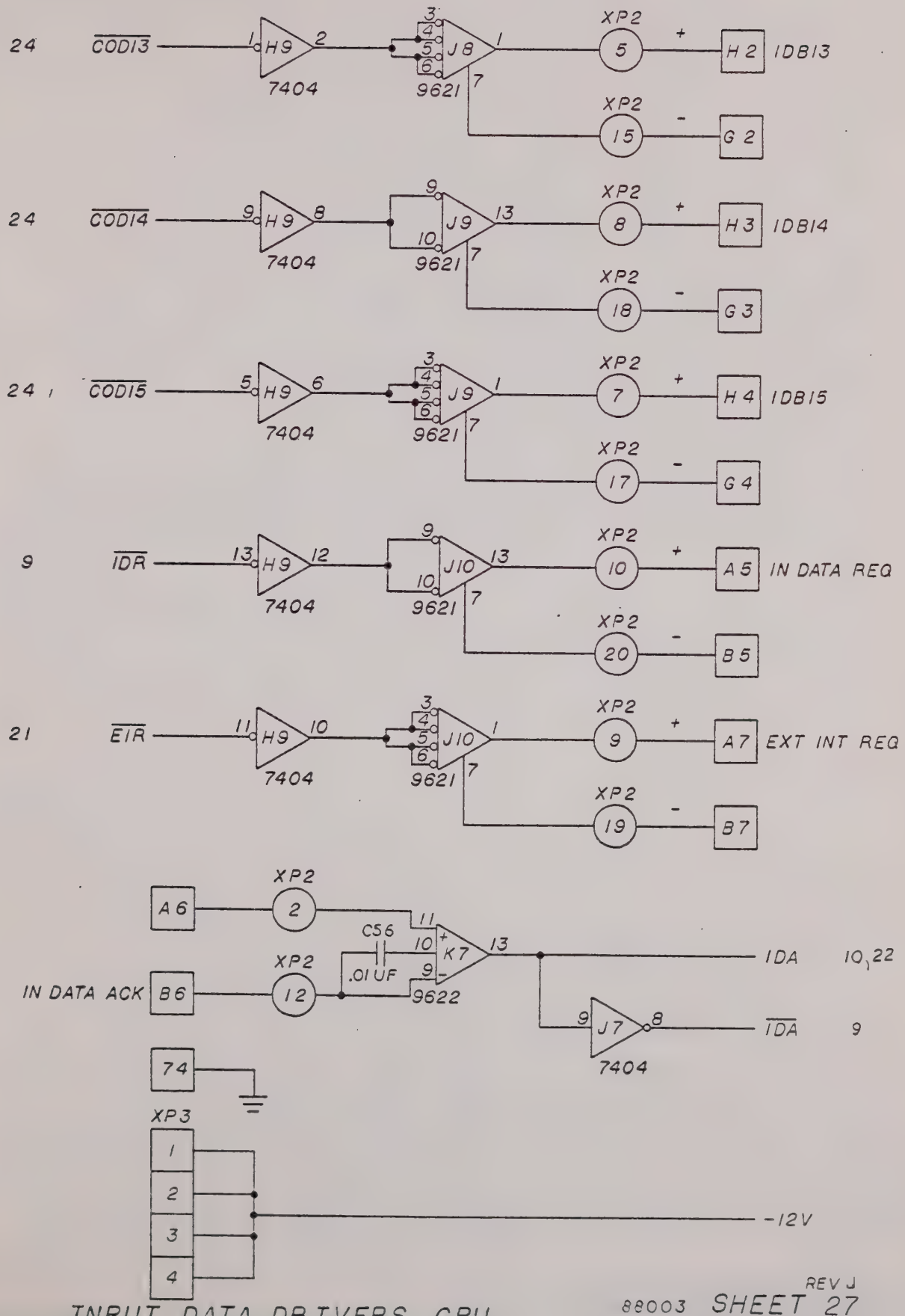


INPUT DATA GATING CPU

REV J
88003 SHEET 24


+5
23 CODOO
L6
7404
L7
9621
XP2
32
+
C1
IDBOO
XP2
22
-
D1
23 CODO1
J7
7404
L7
9621
XP2
31
+
C2
IDBO1
XP2
21
-
D2
23 CODO2
J7
7404
L8
9621
XP2
34
+
C3
IDBO2
XP2
24
-
D3
23 CODO3
J7
7404
L8
9621
XP2
33
+
C4
IDBO3
XP2
23
-
D4
23 CODO4
J11
7404
L11
9621
XP2
35
+
C5
IDBO4
XP2
25
-
D5
23 CODO5
J11
7404
L11
9621
XP2
36
+
C6
IDBO5
XP2
26
-
D6
23 CODO6
J11
7404
K10
9621
XP2
39
+
C7
IDBO6
XP2
29
-
D7


24 CODO7 J11 7404 K10 9621 XP2 40 + C8 IDB07
XP2 30 - D8
24 CODO8 J11 7404 K11 9621 XP2 37 + C9 IDB08
XP2 27 - D9
24 CODO9 J11 7404 K11 9621 XP2 38 + C10 IDB09
XP2 28 - D10
24 CODIO J7 7404 K8 9621 XP2 3 + C11 IDB10
XP2 13 - D11
24 CODII J7 7404 K8 9621 XP2 4 + C12 IDB11
XP2 14 - D12
24 CODI2 H9 7404 J8 9621 XP2 6 + H1 IDB12
XP2 16 - G1



REV J

88003 SHEET 27

INPUT DATA DRIVERS CPU

DATE: 10-31-75

DRAWN:

CHK: J. Weakley 4-13-76

MATERIAL LIST

Datum inc.

JOB NO:

QUANTITY:

REV J

TITLE: UNIVAC MAG TAPE INTERFACE

ASS'Y NO: 88003

SHT1 OF2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	0805-1056	P.C. Board 5001056	DATUM	1			
2	1708-2914	14 Pin Socket - Solder		1	D16		
3	1708-0014	14 Pin Dip Plug (Header)		1	D16		
4	5128-9020	Wire Wrap Stake		92			
5	0302-7410	I.C. 7410		3	A1,H3,L2		
6	0302-7400	7400		8	A2,7,9,B5,C3,H14;K5,J2		
7	0302-0962	862		3	A3,E2,K1		
8	0302-0936	836		14	A4,11,16;B2,15;C1,11;D2,3 D11,15;H15,J3,L1		
9	0302-7402	7402		6	A5,10,H13,J4,5;L3		
10	0302-7404	7404		14	A6,C2,D12-14,E14,H9,H16, J1,7,11;K6,12;L6		
11	0302-0946	846		31	A8,12,15;B3,6,7,12-14,16, C6,7,12-14,16,D6-10;E3,6-8 E10,H6-8,10,J6		
12	0302-7107	74107		13	B1,10,11;C4,E13,15,H2,4, H12;J12,K2,L4,D1		
13	0302-7121	74121		1	B4		
14	0302-7475	7475		4	B8,9;C8,9		
15	0302-7427	7427		6	C5,10;D5,E5,H5,K4		
16	0302-0930	830		1	C15		
17	0302-7425	7425		1	D4		
18	0302-7440	7440		2	E4,K3		
19	0302-7442	7442		1	E11		
20	0302-7174	74174		1	E12		
21	0302-7437	7437	DATUM	2	H1,11		

NOTES:

DF4

DATE: 10-31-75

DRAWN:

CHK: J. Weekley 4-13-76

MATERIAL LIST

datum inc.

JOB NO:

QUANTITY:

REV J

TITLE: UNIVAC MAG TAPE INTERFACE

ASS'Y NO: 88003

SHT 2 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
22	0302-9621	9621	DATUM	10	J8-10,16;K8,10,11;L7,8,11		
23	0302-9622	9622		10	J13-15;K7,13,14,16;L12,13 L16		
24	0302-7430	7430		1	L5		
25	0127-R330	899-5 Resistor Pak	DATUM	2	A13,14		
26							
27	0102-0102	1K Resistor	DATUM	1	R1		
28	0102-0303	30K Resistor		1	R2		
29	0226-0271	270 pf Capacitor		4	C1,4,5,12		
30	0227-0131	130 pf Capacitor		8	C2,7,8,10, ,13,14,16,57		
31	0226-0101	100 pf Capacitor		1	C3		
32	0221-0475	4.7 uf Capacitor		6	C15,22,25,33,34,37		
33	0226-0102-1	.001 uf Capacitor		8	C6,20,26,28,29,30,32,36		
34	0227-0470	47 pf Capacitor		1	C9		
35	0226-0103-3	.01 uf Capacitor		27	C18,19,21,23,24,27,31,35-C38 thru C56		
36	0220-0225	2.2 uf Capacitor	DATUM	1	C17		
37	0227-0331	330 Pf CAPACITOR	DATUM	1	C11		

NOTES:

DF4

datum inc.

1363 S. State College Boulevard, Anaheim, California 92806 • (714) 533-6333 • TWX (910) 592-1289